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(54) **Gate structure of field effect device and method for forming the same**

Gatestruktur einer Feldeffektanordnung und Verfahren zur Herstellung

Structure de grille d'un dispositif à effet de champ et sa méthode de fabrication

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**Description**

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device and a method for forming the same. More particularly, the present invention relates to a thin film transistor applicable to liquid crystal electro-optical devices, contact type image sensors, and the like.

Description of the Prior Art

Insulated gate field effect semiconductor devices known to the present have been widely applied to various fields. Such semiconductor devices comprise a silicon substrate having integrated thereon a plurality of semiconductor elements so that the devices may function as integrated circuits (ICs) and large scale integrated circuits (LSIs).

In addition to the insulated gate field effect semiconductor devices of the type mentioned above, there is another type of such insulated gate field effect semiconductor devices which comprises a thin film semiconductor formed on an insulator substrate, rather than a silicon substrate. Those thin film insulated gate field effect semiconductor devices (referred to hereinafter as TFTS) are now more positively used, for example, in liquid crystal electro-optical devices as switching elements of pixels and driver circuits, and in read-out circuits of contact type image sensors and the like.

Those TFTs are produced, as mentioned above, by laminating thin films on an insulator substrate by a vapor phase process. This process can be conducted in an atmosphere controlled to a temperature as low as about 500°C, or even lower. Moreover, low cost substrates such those made of soda-lime glass and borosilicate glass can be utilized in those TFTs. Thus, the insulated gate field effect semiconductor device of the latter type are advantageous in that they can be fabricated using low cost substrates, and that they can be readily scaled up by depositing the thin films on a substrate having a larger area with the only limiting factor being the dimension of the apparatus in which the thin films are vapor-phase deposited. Accordingly, application of such insulated gate field effect semiconductor devices to liquid crystal electro-optical devices having a large pixel matrix structure or to a one- or two-dimensional image sensors has been expected, and, in fact, a part of such expectations has been met already.

A representative structure for the latter type of TFTs is shown schematically in FIGS. 2 and 6.

Referring to FIG. 2, a typical structure of a conventionally known TFT is explained. In FIG. 2, a thin film semiconductor 2 made of an amorphous semiconductor is deposited on a glass insulator substrate 1, and the thin film 2 comprises on the surface thereof a source area and a drain area 3, source and drain contacts 7, and a gate 11.

Those types of TFTs comprise, as mentioned above, semiconductor layers having deposited by a vapor deposition process. Since the electron and hole mobilities of the semiconductor layers in those TFTs are significantly low as compared with those of the conventional ICs and LSIs, it has been customary to subject the semiconductor layer 2 to a heat treatment for the crystallization thereof.

In a conventional TFT as shown in FIG. 2, the gate 11 is covered with a relatively thick interlayer insulator film 4 such as a silicon nitride film and a silicon oxide film, and to this interlayer insulator film are provided contact holes by a photolithographic process. The source and drain contacts 7 are electrically connected with source and drain areas 3. If feeding points to the source and the drain were to be provided at such positions, the distance L between each of the feeding points and the channel end becomes considerably long.

As mentioned earlier, the TFTs fabricated by a thin film deposition process at low temperatures are significantly low in the carrier mobility. Even upon doping an impurity, the still low conductivity produces a resistance within this distance L. Accordingly, the conventional TFTs suffer poor frequency characteristics and increase in ON circuit resistance. Furthermore, the area necessary for a TFT increases inevitably with increasing length of L. This made it difficult to accommodate a predetermined number of TFTs within a substrate of a limited dimension.

In FIG. 6, a thin film semiconductor 102 composed of an amorphous semiconductor is deposited on a glass insulator substrate 101, and the thin film 102 comprises on the surface thereof a source and a drain area 103, source and drain electrodes 107, and a gate 111.

The TFTs of this type in general are produced by first depositing a semiconductor film on the substrate, and, by patterning, forming island-like semiconductor areas 102 on the desired parts using a first mask. Then, an insulating film and further thereon a gate material are formed, from which a gate electrode 111 and a gate insulating film 106 are obtained by patterning using a second mask. A source and a drain area 103 are established on the semiconductor areas 102 in a self-aligned manner, using the gate electrode 111 and a photoresist formed using a third mask as masks. An interlayer insulator film 104 is formed thereafter. To this interlayer insulator film are provided contact holes using a fourth mask, so that the contacts may be connected to the source and the drain through those contact holes. A contact material is provided to the resulting structure thereafter, which is patterned to form contacts 107 using a fifth mask. Thus is obtained a complete TFT.

Japanese patent application no. JP-A-1183853 describes an insulated gate metal oxide field effect transistor having a side surface of the metal gate anodised to prevent a short circuit between the metal gate and

doped silicon regions.

As can be seen from the foregoing description, a TFT in general requires five masks to complete a structure, and in a complementary TFT, six masks are necessary. Naturally, a more complicated IC should incorporate further more masks. The use of increased number of masks involves a complicated process for fabricating a TFT element, which accompanies frequent mask alignment steps. Such a complicated process inevitably results in a lowered yield and productivity of the TFT elements. The demand for larger electronic devices using the TFT elements, for making the TFT elements themselves more compact, and for finer patterning, makes the yield and productivity even worse. Thus, it has been desired to develop a simpler process which involves no complicated steps, and a TFT based on a novel structure which requires less masks.

## SUMMARY OF THE INVENTION

The present invention aims to provide a semiconductor device based on a novel structure.

It is also desired to provide an insulated gate field effect semiconductor device having each of the feeding points for source and drain in proximity to the channel region at a shorter distance to the channel ends.

Another aim of the present invention is to provide a method for forming semiconductor devices using less masks.

According to one aspect of the present invention, there is provided a method of manufacturing a semiconductor device comprising: forming a semiconductor layer on an insulating surface; forming a gate insulating layer on said semiconductor layer; forming a metal gate electrode on said gate insulating layer; anodic oxidizing side surfaces of said gate electrode to form an anodic oxide layer comprising said gate metal thereon; and introducing dopant impurities into portions of said semiconductor layer in a self-aligned manner with respect to said gate electrode and said oxide layer, thereby forming source and drain impurity doped regions in said semiconductor layer and a channel region therebetween; wherein the formation of said oxide layer provides offset regions in said channel region adjacent said oxide layer, characterised in that said step of anodic oxidizing includes anodic oxidizing upper surfaces of said gate electrode and in that, said method further comprises controlling the size of said offset regions by controlling the thickness of said oxide layer.

According to another aspect of the present invention, there is provided a semiconductor device comprising: a semiconductor layer on an insulating surface, said semiconductor layer comprising source and drain impurity doped regions and a channel region therebetween; a gate insulating layer on said semiconductor layer, a metal gate electrode on said gate insulating layer adjacent to said channel region; an anodic oxide layer comprising said gate metal formed on side surfaces of said gate electrode; wherein said channel region includes offset regions adjacent said anodic oxide layer, said anodic oxide layer being also formed on upper surfaces of said gate electrode and the size of said offset regions being determined by the thickness of said oxide layer.

A feature of an insulated gate field effect semiconductor device embodying the present invention is that the TFT comprises a metal gate electrode having a film of an anodically oxidized gate electrode material provided on upper and side surfaces thereof. Another feature of an insulated gate field effect semiconductor device embodying the present invention is that contact holes for the extracting contacts of the source and drain semiconductor regions are provided at about the same position of the end faces of the anodically oxidized film established at the sides of the gate electrode.

To improve the carrier mobility in the semiconductor layer, if necessary, the substrate having deposited thereon a silicon semiconductor film containing hydrogen therein may be subjected to thermal treatment to thereby modify said semiconductor film into such having a crystalline structure. Furthermore, to minimize the distance L between the feeding points and the channel ends, the metal gate electrode is provided, e.g., an aluminum gate electrode, and the outer (peripheral portion) of this gate electrode is oxidized to form on the side thereof a metal oxide film, e.g., an aluminum oxide film.

Furthermore, the gate electrode together with the aluminum oxide film surrounding said gate electrode may be used as a mask to form contact holes for the extract contacts of the source and the drain with a side surface of the contact hole located substantially on a side surface of the aluminum oxide film in a self-aligned manner. An embodiment of the present invention provides, as is shown in the schematic cross sectional view of FIG. 1, a TFT comprising a metal gate electrode 8 having on upper and side surfaces thereof an oxide layer 10 comprising the metal, e.g. an aluminum oxide layer, to which source and drain electrodes 7 (contacts for a drain and a source) connected to the source and drain semiconductor regions respectively are provided approximately at the end of the oxide layer. The source and drain electrodes 7 are connected to the source and drain semiconductor regions 3. By taking such a construction, a shorter distance L between said feeding points and the channels has been achieved. In Fig. 1, a channel is located adjacent to the gate electrode 8 between the source and drain semiconductor regions 3 under a gate insulating film 6. In Fig.1, the gate insulating film 6 is provided between the channel and the gate electrode 8. In Fig. 1, a side of at least one of the source and drain electrodes 7 is substantially aligned with a side of the oxide layer 10. In Fig.1, the oxide layer is in contact with the gate electrode and at least one of the source and drain electrodes. In Fig. 1, a side of the source semiconductor region is aligned with a side of the oxide layer and also a side of the drain semiconductor region is aligned with a side of the oxide layer.

Ideally, it is favorable to reduce the distance L to zero from the viewpoint of lowering the resistance (in FIG. 1, indeed, the distance L is approximately zero). However, difficulties ascribed to process technology, for example, a small extension of the source and the drain semiconductor regions under the gate, hinder achievement of a complete zero. Nevertheless, a shorter distance L still promises a considerable effect in reducing the resistance.

In the embodiment exemplified by FIG. 1, the aluminum oxide film around the gate electrode is established over the side and the upper plane of the gate electrode, i.e., over the whole outer plane exposed to the outside. The provision of the aluminum oxide film over the side of the gate electrode advantageously shortens the distance L. As the aluminum oxide film is provided to the whole outer surface as is shown in FIG. 1, this film can be used as it is as a part of a mask at the fabrication of the contact holes, because the aluminum oxide film is hardly etched. Furthermore, other wiring, e. g., a wiring for the source electrode, may be crossed over this aluminum oxide film to establish a three-dimensional wiring which facilitates the later process steps for integration.

In an insulated gate field effect semiconductor device embodying the present invention, what is meant by providing the contact holes for the extract contacts of the source and the drain in an approximately the same position as that of the ends of the gate electrode and the aluminum oxide film, is a structure resulting upon formation of contact holes in a self-aligned manner using the ends of the gate electrode and the aluminum oxide film, as well as a structure having a slight positional deviation in the case of using masks at the positioning, ascribed to the incomplete alignment of the masks. Referring to FIG. 1, for example, the edge portion of the insulator film 9 is sometimes displaced from the end of the aluminum oxide at the mask alignment when the contact portion alone is intended to form. Such a case is included in the latter case mentioned hereinbefore. In the former case taking advantage of the aluminum oxide film as a mask, i.e., in the case of extending the etching area of the insulator film up to the gate, the insulator film 9 can be completely removed from the gate, and the end of the source or the drain is certainly aligned with that of the aluminum oxide film 10 to result in a shortened distance L.

The aluminum oxide may be provided around the gate electrode by anodically oxidizing said gate electrode. The anodic oxidation process comprises applying an electric current to a metal gate electrode having dipped in an acidic solution to oxidize the surface thereof by an electrochemical reaction. There may be used other processes, provided that the oxide film has a dense structure and that the oxidation can be effected rapidly.

Another feature of an insulated gate field effect semiconductor device embodying the present invention is that it comprises a TFT gate electrode surrounded by an anodically oxidized film of the same material constituting the gate electrode, with the contacts (source and drain electrodes) connected to the source and the drain being brought into contact with the upper planes and the sides of the source and the drain each, and that the contacts (source and drain electrodes), connected to each of the drain and the source regions, extend on the upper surface of the oxidized film surrounding said gate electrode.

As shown in the schematically shown cross sectional view of FIG. 5, a TFT embodying the present invention comprises an anodically oxidized film 110 at least as the surroundings of the gate electrode 108 comprising a metal, with the upper planes and the sides of the source and drain semiconductor regions slightly sticking out from the ends of said anodically oxidized film. The source and drain semiconductor regions are connected to the contacts 107 (source and drain electrodes) through these slightly sticking out portions (that is, the upper planes and the sides of the source and drain semiconductor regions) to make the area of connection larger. Furthermore, the contacts 107 are extended over the upper portion of the anodically oxidized film 110, at which they are patterned into separate electrodes. In Fig. 5, a channel is located adjacent to the gate electrode 108 between the source and drain semiconductor regions 103 under a gate insulating film 106. In Fig.5, the gate insulating film 106 is provided between the channel and the gate electrode 108. In Fig.5, said anodically oxidized film 110 is provided between the gate electrode 108 and the source and drain electrodes 107.

Referring to FIG. 7, a fabrication process for the TFT according to an embodiment of the present invention and having the structure illustrated in FIG. 5 is explained. The FIG. 7 is provided as an explanatory means and the details concerning dimension and shape are a little different from those of the actual device.

First, as in FIG. 7 (A), on a glass substrate, e. g., a substrate of a heat-resistant crystallized glass 101, is deposited a semiconductor layer 102. The semiconductor layer, e. g., a silicon semiconductor layer, may be an amorphous semiconductor, a polycrystalline semiconductor, or any other selected from a wide variation, and may be deposited by processes such as a plasma-assisted CVD (chemical vapor deposition), sputtering, and pyrolytic CVD, depending on the type of the semiconductor used. In the following explanation, the process steps are described according to a case in which a polycrystalline silicon semiconductor is used. The next step in the fabrication process comprises forming a silicon oxide film 106 on the semiconductor layer 102, so that the silicon oxide film 106 may function as the gate insulating film. Further on the silicon oxide film is formed an contact material layer, an aluminum layer in this case, from which a gate electrode is established. The contact material layer is then patterned into the gate electrode 108 using a first mask (21). An anodically oxidized film is provided as a surrounding of the gate electrode 108, by

conducting an anodic oxidation in an electrolyte for the anodic oxidation. A pore-free aluminum oxide 110 can be provided at least at the vicinity of the channel region to the surrounding of the gate electrode, as illustrated in FIG.7 (B).

The electrolyte to be used in the anodic oxidation includes, representatively, strong acid solutions of, such as sulfuric acid, nitric acid, and phosphoric acid, as well as mixed acid comprising tartaric acid or citric acid, having added therein ethylene glycol or propylene glycol or the like. The solution (electrolyte) may be further mixed with a salt or an alkaline solution to adjust the solution (electrolyte) for the pH value.

The anodic oxidation was performed as follows. The substrate was immersed into an AGW electrolyte having prepared by adding 9 parts of propylene glycol to 1 part of an aqueous 3% tartaric acid solution. A direct current (D.C.) was applied to the substrate by connecting the aluminum gate to the anode of a power source and using a platinum cathode as the counter electrode. The electric current was applied first at a constant current density of 3 $mA/cm^2$ for 20 minutes, and then at a constant voltage for 5 minutes, to thereby obtain a 1,500 Å thick aluminum oxide film around the gate electrode. The insulating properties of this aluminum oxide film was evaluated using a specimen having subjected to an oxidation treatment under the same condition as that employed above. As a result, a resistivity of $10^{15}\ \Omega$ and a dielectric breakdown of $3 \times 10^6$ V/cm was obtained for the film. The surface of the sample was observed through a scanning electron microscope to find surface irregularities at a magnification of about 10,000, but no minute holes. The film was therefore evaluated as a favorable insulator coating.

On the surface of the thus obtained insulator film was further deposited a silicon oxide film 112 by plasma-assisted CVD. The film was then anisotropically etched along a direction nearly vertical to the substrate to leave over silicon oxide 113 on the side walls of the protrusion constructed by the gate electrode and the anodically oxidized film (see FIG. 7(D)). The semiconductor layer 102 is then removed by etching in a self-aligned manner using the remaining silicon oxide film 113, and the gate electrode 108 and the anodically oxidized film 110 of the protrusion as a mask. The resulting structure is shown in FIG. 7(E). The structure as viewed from the upper side is shown in FIG. 8(A). The cross sectional view taken along the line A-A' indicated in FIG. 8(A) is given in FIG. 7.

The structure as shown in FIG. 7(E) was subjected to a selective etching to remove only silicon oxide, i.e., the silicon oxide film 113 and the gate insulating film, using the gate electrode 108 and the anodically oxidized film 110 thereof as the mask, to thereby obtain a structure having a part of the semiconductor layer 102 exposed to outside at the edge of the gate, as shown in FIG. 7(F) and FIG. 8(B).

The resulting semiconductor portion exposed to the air is then doped with impurities to establish a source and a drain. As can be seen in FIG. 7(F), the part exposed to the air was bombarded with phosphorus ions from the upper side of the substrate using the anodically oxidized film 110 of the gate electrode as the mask. Thus are formed the source and drain regions 103. In Fig.7 (F), sides of the source and drain regions 103 are located at sides of the semiconductor portion exposed to the air. For the activation of the regions, a laser beam is irradiated to the exposed portions. Instead of carrying out the laser annealing as the activation treatment of the source and the drain regions, they can be otherwise activated by thermal annealing and the like.

An aluminum layer is then formed on the upper surface of the resulting structure, which is separated into source and drain electrodes by etching the aluminum layer into a predetermined pattern using a second mask (22) . The structure obtained in this step is shown in FIG. 8(C). This structure is then finished into a TFT shown in FIGS. 7(G) and 8(D), by removing the unnecessary portions of the semiconductor layer 102 using the source and the drain electrodes 107 and the anodically oxidized film 110 on the gate electrode as the mask.

It can be seen from the foregoing description that an embodiment of the present invention provides a TFT by involving merely 2 masks.

In the case of a complementary TFT, 1 or 2 more masks suffice the fabrication of the structure.

The TFT thus obtained can be connected to the outer through a non-oxidized part of the gate electrode left out at the anodic oxidation, by carrying out the anodic oxidation treatment with care not to contact the part of the gate electrode with the electrolyte used at the anodic oxidation, or through a non-oxidized part of the gate electrode produced by selectively etching the anodically oxidized film exposed to the outer at the final step of selective etching of the source and drain electrodes together with the accompanying anodically oxidized film, after etching the unnecessary semiconductor layer. Otherwise, a contact hole may be perforated in a specific anodically oxidized film, using a third mask.

The foregoing description for the fabrication of a TFT is merely an example, and it should be understood that the present invention is not limited thereto. For example, the source and the drain regions may be doped with impurities by ion-bombardment at the stage shown in FIG. 7(B) using the anodically oxidized film 110 of the gate electrode as the mask, instead of carrying out the doping step after the patterning of the semiconductor layer 102 as demonstrated above in FIG. 7(F).

Furthermore, after the semiconductor layer 102 is established and before forming a gate, another photomask can be incorporated to carry out patterning of the semiconductor layer at the proximity of the TFT area into an island-like structure. Thus can be obtained a structure as shown in FIG. 9, which comprises only the substrate or an insulator film established on the substrate

under the lead wiring instead of the semiconductor layer 102. Such a configuration avoids establishment of a capacitor which may otherwise be formed by the gate wiring and a semiconductor layer. In this manner can a TFT of an increased response be fabricated by using only 3 masks. The structure as viewed from the upper side is given in FIG. 9(A), and the cross sectional view along the line B-B' is given in FIG. 9(B).

In a general structure for an insulated gate field effect semiconductor device embodying the present invention as shown in FIG. 5, the end of the gate is displaced from the position of the end of the source or the drain region by the thickness of the insulator film (anodically oxidized film) provided around the gate. Such an offset structure decreases the carrier density at the channel and, at the same time, reduces the electric field intensity at the drain-channel junction that the drain breakdown voltage can be improved. Since the thickness of the insulator film may be varied in the range of, for example, from 10 to 50 nm by changing the condition at the oxidation, the amount of this offset can be readily set as desired, depending on the required device characteristics. Furthermore, a lightly doped drain (LDD) structure can be realized by controlling the impurity concentration of this offset portion to a value lower than that in the source and the drain regions.

In Fig.5, a channel length (a distance between the source and the drain regions) is longer than a length of the gate electrode in a direction of the channel length.

An offset region to which no electric field or very weak electric field is applied by a gate voltage can be formed in a portion of a channel region in contact with a source or a drain region in an insulated gate field effect transistor in which a channel length thereof is longer than a length of a gate electrode thereof in a direction of the channel length. For example, in Fig.5, no electric field is applied to the offset region located in the channel region in the semiconductor 102 between a portion of the channel region just under the gate electrode 108 and the source or the drain region, a very weak electric field is applied to the offset region as compared with an electric field applied to the portion of the channel region just under the gate electrode 108. In Fig.5, for example, the channel length is longer than the length of the gate electrode 108 in the direction of the channel length by an approximately twofold thickness of the insulator film (anodically oxidized film).

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 shows a schematically drawn cross sectional view of an insulated gate field effect semiconductor device according to an embodiment of the present invention;

FIG.2 shows a schematically drawn cross sectional view of a conventional insulated gate field effect semiconductor device;

FIG.3 shows a fabrication process of an insulated gate field effect semiconductor device according to an embodiment of the present invention;

FIG. 4 shows a circuit diagram of a liquid crystal electro-optical device to which an insulated gate field effect semiconductor device according to an embodiment of the present invention is applied;

FIG. 5 shows the structure of a TFT according to an embodiment of the present invention;

FIG. 6 shows the structure of a conventional TFT;

FIG. 7 shows a schematically shown cross sectional view of a TFT embodying the present invention to illustrate the fabrication step thereof;

FIG. 8 shows a schematically shown view seen from the upper side of a TFT embodying the present invention to illustrate the fabrication step thereof;

FIG. 9 shows the structure of another TFT embodying the present invention;

FIG. 10 shows a schematically drawn circuit diagram of a liquid crystal electro-optical device to which a complementary TFT according to an embodiment of the present invention is applied;

FIG. 11 shows a schematically drawn cross sectional view illustrating a fabrication process of a liquid crystal electro-optical device to which a complementary TFT according to an embodiment of the present invention is applied;

FIG. 12 shows a schematically drawn diagram indicating the mounted arrangement on the substrate of a liquid crystal electro-optical device to which a complementary TFT according to an embodiment of the present invention is applied;

FIG. 13 shows a schematically drawn circuit diagram of a liquid crystal electro-optical device to which a complementary TFT according to another embodiment of the present invention is applied; and

FIG. 14 shows a schematically drawn diagram indicating the mounted arrangement on the substrate of a liquid crystal electro-optical device to which a complementary TFT according to another embodiment of the present invention is applied.

## DETAILED DESCRIPTION OF THE EMBODIMENTS

Now embodiments of the present invention are described in further detail below referring to some EXAMPLES, however, it should be noted that the present invention is not to be construed as being limited thereto.

### EXAMPLE 1

Referring to FIG. 4, an example in which a TFT embodying the present invention is applied to a liquid crystal electro-optical device having a diagram as illustrated in Fig.4 is described. In FIG. 4, an N-channel TFT (N-TFT) 22 and a P-channel TFT (P-TFT) 21 in a complementary configuration are provided to each of the pixels of the liquid crystal device. Each of the TFTS are connected to a common signal wire 50 through respective

gate electrodes, and the output terminals of the N-TFT 22 and the P-TFT 21 are connected to the common pixel electrode 43, whereas each of the other output terminals 28 and 35 in the respective TFTs is connected to the other signal wires 52 and 53 to provide an inverter structure. The positions of the P-TFT and the N-TFT may be reversed to establish a buffer structure and provide the complementary TFTs to each of the pixel electrodes.

Referring to FIGS. 3(A) to 3(G), the fabrication process of a complementary TFT (C/TFT) on a substrate embodying the present invention to be used in a liquid crystal electro-optical device is described below.

In FIG. 3(A), a silicon oxide film from 1000 to 3000 Å in thickness as a blocking layer 24 was deposited by radio-frequency (RF) magnetron sputtering on a non-expensive glass substrate 1 which is resistant to a heat treatment at a temperature of 700°C or lower, e.g. about 600°C. Examples of such glasses useful as the substrate include crystallized glass such as AN glass and neo-ceramic glass, and Vycor® 7913 (a heat resistant glass manufactured by Corning Corp.).

The silicon oxide film was deposited in a 100% oxygen atmosphere at the deposition temperature of 150°C, at an output of from 400 to 800 W and a pressure of 0.5 Pa. The target used was quartz or single crystal silicon, and thus was obtained the film at a film deposition rate of from 30 to 100 Å/minute.

An amorphous silicon film was deposited on the silicon oxide blocking layer by any of the processes of low pressure chemical vapor deposition (LPCVD), sputtering, and plasma-assisted CVD (PCVD).

In the LPCVD process, film deposition was conducted at a temperature lower than the crystallization temperature by 100 to 200°C, i.e., in the range of from 450 to 550°C, e.g., at 530°C, by supplying disilane ($Si_2H_6$) or trisilane ($Si_3H_8$) to the CVD apparatus. The pressure inside the reaction chamber was controlled to be maintained in the range of from 30 to 300 Pa. The film deposition rate was 50 to 250 Å/minute. Furthermore, optionally boron may be supplied as diborane during the film deposition to control the threshold voltage ($V_{th}$) of the N-TFT to be approximately the same as that of the P-TFT.

The film deposition process by sputtering was conducted using a single crystal silicon as the target in an argon atmosphere having added therein from 20 to 80% of hydrogen, e.g., in a mixed gas atmosphere containing 20% of argon and 80% of hydrogen. The back pressure prior to sputtering was controlled to $1 \times 10^{-5}$ Pa or lower. The film was deposited at a film deposition temperature of 150°C, a frequency of 13.56 MHz, a sputter output of from 400 to 800 W, and a pressure of 0.5 Pa.

In the deposition of a silicon film by a PCVD process, the temperature was maintained, e.g., at 300°C, and monosilane ($SiH_4$) or disilane ($Si_2H_6$) was used as the reacting gas. A high frequency electric power was applied at 13.56 MHz to the gas inside the PCVD apparatus to effect the film deposition.

The films thus obtained by any of the foregoing processes preferably contains oxygen at a concentration of $5 \times 10^{21}$ $cm^{-3}$ or lower, and more preferably, $7 \times 10^{20}$ $cm^{-3}$ or lower. If the oxygen concentration is too high, the film thus obtained would not crystallize. Accordingly, there would be required to elevate the thermal annealing temperature or to take a longer time for the thermal annealing. Too low an oxygen concentration, on the other hand, increases an off-state leak current due to a backlighting when the semiconductor layer is irradiated with a light beam in a liquid crystal electro-optical device. Accordingly, the oxygen concentration was set in the range of from $4 \times 10^{19}$ to $4 \times 10^{21}$ $cm^{-3}$ to readily crystallize the semiconductor layer by thermal annealing at a moderate temperature (600°C or lower). The hydrogen concentration was $4 \times 10^{20}$ $cm^{-3}$, which accounts for 1 % by atomic with respect to the silicon concentration of $4 \times 10^{22}$ $cm^{-3}$.

Oxygen concentration was controlled to $7 \times 10^{20}$ $cm^{-3}$ or lower, preferably $7 \times 10^{19}$ $cm^{-3}$ or lower, and more preferably $1 \times 10^{19}$ $cm^{-3}$ or lower to enhance crystallization of the source and drain regions, while selectively adding oxygen, carbon, or nitrogen by ion-implantation to a part of the channel forming regions of the TFT which constitute the pixel, to such an amount to give a concentration in the range of from $5 \times 10^{19}$ to $5 \times 10^{21}$ $cm^{-3}$, preferably $5 \times 10^{20}$ to $5 \times 10^{21}$ $cm^{-3}$ to reduce the sensitivity to light. In a TFT fabricated in this manner, particularly in the TFT which constitutes the peripheral circuits, the oxygen concentration was lowered while a higher carrier mobility was imparted. This facilitated high frequency operation while the leak current of the TFTs at the OFF state in the pixel peripheral switching elements is reduced.

Thus was deposited an amorphous silicon film at a thickness of from 500 to 5,000 Å, e.g., at a thickness of 1,500 Å. The amorphous silicon film was then heat-treated at a moderate temperature in the range of from 450 to 700°C for a duration of from 12 to 70 hours in a non-oxidizing atmosphere. More specifically, for example, the film was maintained at 600°C under a hydrogen or nitrogen atmosphere.

Since on the surface of the substrate was provided an amorphous silicon oxide layer under the silicon film, the whole structure could be uniformly annealed because there generated no nucleus present during the heat treatment. That is, the silicon film during deposition maintains an amorphous structure, and hydrogen is present only as a free atom.

Then, at the annealing step, the silicon film undergoes phase transition from the amorphous structure to a structure having a higher degree of ordering, and partly develops a crystalline portion. Particularly, the region which attained a relatively high degree of ordering at the film deposition of silicon tend to crystallize at this stage. However, the silicon bonding which combines the silicon atoms to each other attracts an atom in a region to another in another regions. This effect can be observed by

a laser Raman spectroscopy as a peak which is shifted to a lower frequency side as compared with the peak at 522 $cm^{-1}$ for a single crystal silicon. The apparent grain size can be calculated by the half width as 50 to 500 Å, i.e., a size corresponding to that of a microcrystal, but, in fact, the film has a semi-amorphous structure comprising a plurality of those highly crystalline regions yielding a cluster structure, and the clusters are anchored to each other by the bonding between the silicon atoms (clustering). Thus was obtained a film having a semi-amorphous structure.

The semi-amorphous film thus obtained was subjected to a measurement of the elemental distribution along the direction of the depth, using, for example, a secondary ion mass spectroscopy (SIMS). The minimum concentration for the dopants (impurities) was found (either at the surface or at an inner portion apart from the surface) 3.4 x $10^{19}$ $cm^{-3}$ for oxygen and 4 x $10^{17}$ $cm^{-3}$ for nitrogen. Hydrogen was found at a concentration of 4 x $10^{20}$ $cm^{-3}$, which accounts for 1 % by atomic with respect to silicon which is present at a concentration of 4 x $10^{22}$ $cm^{-3}$. The crystallization could be achieved, for example, by a thermal treatment at 600°C for a duration of 48 hours in the case of a 1000 Å thick film containing oxygen at a concentration of 3.5 x $10^{19}$ $cm^{-3}$. Upon increasing the oxygen concentration of the film to 3 x $10^{20}$ $cm^{-3}$ and considering the film thickness, it was possible to crystallize a film as thick as in the thickness range of from 0.3 to 0.5 µm by annealing at 600°C. However, a film having the same oxygen concentration but reduced in thickness to 0.1µm required a heat treatment at a higher temperature of 650°C for the crystallization. In short, a thicker film and a lower impurity (e.g., oxygen) concentration favored the crystallization.

The semi-amorphous film thus obtained yields, as a result, a state in which substantially no grain boundary (referred to hereinafter as GB) exists. Since the carrier easily moves between the clusters through the anchored portions, a carrier mobility far higher than that of a polycrystalline silicon having a distinct GB can be realized. More specifically, a hole mobility, µh, in the range of from 10 to 200 $cm^2/V{\cdot}sec$ and an electron mobility, µe, in the range of from 15 to 300 $cm^2/V{\cdot}sec$, are achieved.

On the other hand, if a high temperature annealing in the temperature range of from 900 to 1200°C were to be applied in the place of a moderate temperature annealing as described hereinabove, impurities undergo a solid phase growth from the nuclei and segregate in the film. This results in the high concentration of oxygen, carbon, nitrogen, and other impurities at the GB which develops a barrier. Thus, despite the high mobility within a single crystal, the carrier is interfered at its transfer from a crystal to another by the barrier at the GB. In practice, it is quite difficult to attain a mobility higher than or equal to 10 $cm^2/V{\cdot}sec$ with a polycrystalline silicon at the present.

Thus, in the present EXAMPLE embodying the present invention, a semi-amorphous silicon semiconductor is utilized. Otherwise, a polycrystalline silicon semiconductor can be utilized, provided that a sufficiently high carrier mobility therein can be achieved therein.

Referring to FIG. 3(A), a process for fabricating an area 21 (having a channel width of 20 µm) for a P-TFT and an area 22 for an N-TFT at the right and left hand side, respectively, of FIG. 3(A) is described. The silicon film was masked with a first photomask①, and subjected to photo-etching to obtain the areas.

On the resulting structure was deposited a silicon oxide film as a gate insulating film 27 to a thickness of from 500 to 2,000 Å, e.g., to a thickness of 1,000 Å. The conditions for the film deposition were the same as those employed in depositing the silicon oxide film to give a blocking layer. Further, a small amount of a halogen such as fluorine may be added during the film deposition to fix sodium ions.

Further on the gate insulating film was deposited an aluminum film at a thickness of 0.3 µm, which was subjected to patterning using a second photomask② Then, a gate 26 for the P-TFT and another gate 25 for the N-TFT were fabricated. The channel length was, for example, 10 µm.

In FIG. 3(C), a photoresist 31 was formed using a photomask③, and then boron was doped to a source 28 and a drain 30 for P-TFT at a dose of 1 x $10^{15}$ $cm^{-2}$, by ion implantation.

Similarly, a photoresist 32 was formed using a photomask④, and then phosphorus was doped to a source 35 and a drain 33 for N-TFT at a dose of 1 x $10^{15}$ $cm^{-2}$, by ion implantation.

The doping was conducted through the gate insulating film 27. However, as is shown in FIG. 3(B), the silicon oxide on the silicon film may be removed using the gate electrodes 25 and 26 as the masks, and then boron and phosphorus may be directly doped into the silicon film by ion implantation.

After removing the photoresist 32, the structure was reheated at 650°C for a duration of 10 to 50 hours for annealing. Thus the impurities in the source 28 and the drain 30 of the P-TFT, as well as those in the source 35 and the drain 33 of the N-TFT were activated to give $P^+$ and $N^+$.

Furthermore, channel forming regions 34 and 29 were provided as a semi-amorphous semiconductor or a polycrystalline semiconductor under the gate electrodes 25 and 26.

As described in the foregoing, a C/TFT can be fabricated in a self-aligned manner without heating it to a temperature of 700°C or higher. This allows use of a non-expensive substrates and excluding use of the expensive quartz substrate and the like. The process is therefore suitable for manufacturing liquid crystal display devices having many pixels. The thermal annealing was conducted twice, as shown in FIGS. 3(A) and 3(D). However, the annealing corresponding to that of FIG. 3 (A) may be omitted depending on the required device

characteristics, and the thermal annealing may be integrated into one corresponding to that of FIG. 3(D) to speed up the process.

In the present EXAMPLE, aluminum was used for the gate. This was effective for reducing the interface state density of the gate insulating film and also the loss of carriers, because at the annealing step corresponding to FIG. 3(D), the aluminum functioned effectively for dissociating hydrogen molecules incorporated in the gate insulating film into hydrogen atoms.

In the step corresponding to FIG. 3(E), the gate electrodes 25 and 26 were anodically oxidized to cover the surfaces thereof with aluminum oxide. More specifically, the substrate was dipped into a 13.7 % sulfuric acid bath, and to the substrate was applied a current at a density of 1 $mA/cm^2$ using a carbon anode placed at a distance of 30 cm from the substrate. Thus was formed aluminum oxide film at a thickness of from 0.2 to 1 μm, for example, at a thickness of 0.5 μm.

The solution to be used in the anodic oxidation include, representatively, strong acid solutions of, such as sulfuric acid, nitric acid, and phosphoric acid, as well as mixed acid comprising tartaric acid or citric acid, having added therein ethylene glycol or propylene glycol or the like. A salt or an alkaline solution may be further added to the solution to thereby adjust the pH value of the solution.

The anodic oxidation was performed as follows. The substrate was immersed into an AGW electrolyte having prepared by adding 9 parts of propylene glycol to 1 part of an aqueous 3% tartaric acid solution. A direct current (D.C.) was applied to the substrate by connecting the aluminum gate electrode to the anode of a power source and using a carbon cathode as the counter electrode.

The electric current was applied first at a constant current density of 1 $mA/cm^2$ for 20 minutes, and then at a constant voltage for 5 minutes, to thereby obtain a 5,000 Å thick aluminum oxide film around the gate electrode. The insulating properties of this aluminum oxide film was evaluated using a specimen having subjected to an oxidation treatment under the same condition as that employed above. As a result, a resistivity of $10^9$ Ω-m and a dielectric breakdown of $2 \times 10^5$ V/cm was obtained for the film.

The surface of the sample was observed through a scanning electron microscope to find surface irregularities at a magnification of about 8,000, but free of minute holes. The film was therefore evaluated as a favorable insulator coating.

In the step corresponding to FIG. 3(F), the interlayer insulator 41 was formed by depositing a silicon oxide film by sputtering mentioned hereinbefore. Alternatively, the silicon oxide film may be deposited using an LPCVD or a photochemical vapor deposition method. The silicon oxide film thus obtained was 0.2 to 1.0 μm thick. Then, as is also shown in FIG. 3(F), a contact hole 42 was perforated in the film using a photomask ⑤ This fabrication process is characterized by that a reactive ion etching (RIE) process was employed to perforate the contact hole 42 at a position as near as possible to the channel, using gate electrodes 25 and 26 and the aluminum oxide film around them in a self-aligned manner, and thus minimizing the distance L between the channel and the feeding points for the source and the drain.

Then, aluminum was deposited over the whole structure by sputtering at a thickness of 0.5 to 1.0 μm, and leads 52 and 53 were formed using a photomask ⑥. These leads were used as contacts for the source regions 28 and 35 of the P-TFT and the N-TFT as shown in FIG. 3(G).

The surface of the resulting structure was coated with an organic resin 44, e.g., a transparent polyimide resin for smoothening, and subjected again to perforation of contact holes using a photomask ⑦.

As is shown in FIG. 3(G), two TFTs were brought into a complementary arrangement, and an output terminal thereof was connected to a transparent electrode 43 provided to one side of a pixel of a liquid crystal device. The transparent electrode 43 was fabricated by etching an indium tin oxide (ITO) film having established by sputtering, using a photomask ⑧ at the etching. The ITO film was such having deposited in a temperature range of from room temperature to 150°C, followed by annealing at 200 to 400°C in oxygen or in the atmosphere. Thus was fabricated a structure comprising the P-TFT 21, the N-TFT 22, and the transparent electrode 43 made of a conductive film on a single glass substrate 1.

The TFT thus obtained comprises a P-TFT having a mobility of 20 $cm^2/V$ sec with a $V_{th}$ of -5.9 V, and an N-TFT having a mobility of 40 $cm^2/V$sec with a $V_{th}$ of +5.0 V.

It can be seen from the foregoing description that a mobility far higher than a value generally believed for a TFT has been achieved. This has enabled for the first time the production of an active matrix liquid crystal display device using a C/TFT pair for each of the pixels of the liquid crystal electro-optical device. Furthermore, the present embodiment has also enabled formation of the peripheral circuits on-glass, i.e., by fabricating the circuits on the same substrate employing a fabrication process similar to that applied to the fabrication of the TFTs.

In the EXAMPLE, the TFT embodying the present invention was applied to a liquid crystal electro-optical device. Because of the excellent frequency characteristics of the TFTs, such liquid crystal electro-optical devices can easily display dynamic images, and are therefore suitable for applications such as projection TV sets, view finders of video movies, and hanging-type TV sets. Additional application field to be mentioned is the driving elements of one- and two-dimensional image sensors, in which the excellent frequency characteristic is taken full advantage of in the rapid reading that can fully respond to the G4 standard.

A cell for a liquid crystal electro-optical device can be fabricated by a process well known in the art, using a pair of glass substrates, one having fabricated in a manner described above and the other having established thereon counter electrodes composed of transparent electrodes provided in stripes. The glass cell is filled with a liquid crystal material.

If a twisted nematic (TN) liquid crystal were to be used, the cell spacing should be controlled to be about 10 µm, and orientation control films formed by rubbing treatment should be provided on the both of the transparent conductive films.

If a ferroelectric liquid crystal (FLC) were to be used as the liquid crystal material instead, the operating voltage should be controlled to ± 20 V, the cell spacing should be controlled to 1.5 to 3.5 µm, e.g., 2.3 µm, and the orientation control film should be formed only on the counter electrode by subjecting the film to rubbing treatment.

In the case a dispersion type liquid crystal or a polymer liquid crystal is used, an orientation control film can be omitted and the operation voltage should be controlled to ±10 to ±15 V and the cell spacing to 1 to 10 µm to increase the switching rate.

Since the polarizer sheet can be excluded particularly in the case a dispersion type liquid crystal is used, the cell can be used either as a reflection type or as a transmission type and have an increased quantity of light. Moreover, because the liquid crystal has no threshold, the use of the C/TFT embodying the present invention having a distinct threshold voltage enables a device having a higher contrast and free of cross-talk (undesired interference between the neighbouring pixels).

EXAMPLE 2

Referring to FIG. 10, an example of an active matrix type liquid crystal electro-optical device to which a TFT embodying the present invention is applied is described. FIG. 10 shows the circuit diagram of the liquid crystal electro-optical device, and it can be seen therefrom that the active elements of the present EXAMPLE are provided in a complementary arrangement having a P-TFT and an N-TFT per one pixel contact.

The actual arrangement of the contacts and the like corresponding to the circuit shown in FIG. 10 is given, in FIG. 12. For brevity's sake, merely a part of the circuit corresponding to a 2 x 2 matrix is given in FIG. 12.

Referring first to FIG. 11, the process for fabricating the substrate for use in the liquid crystal electro-optical device embodying the present invention is described. FIG. 11(A) shows a step of depositing silicon oxide film as a blocking layer 151 at a thickness of from 1000 to 3000 Å, on a non-expensive glass substrate 150 using RF magnetron sputtering. In this case, the glass substrate is made of a non-expensive glass which resists to a heat treatment at 700°C or lower, e.g., at about 600°C. The conditions for the fabrication are the same as those used in EXAMPLE 1. An amorphous silicon film was formed on the blocking layer at a thickness of 500 to 3000 Å, e.g. 1500Å in the same way as in the EXAMPLE 1. Then, the amorphous silicon film was annealed in, for example, hydrogen atmosphere at 600°C for a duration of 12 to 70 hours.

The amorphous silicon film turned into a phase having a higher structural ordering upon annealing, comprising partly a crystalline portion. The resulting film had a hole mobility, µh, of from 10 to 200 $cm^2/V \cdot sec$, and an electron mobility, µe, of from 15 to 300 $cm^2/V \cdot sec$.

As is shown in FIG. 11(A), the silicon film was subjected to a photoetching treatment using a first photomask ⑪ to establish a P-TFT area 130 (having a channel length of 20 µm) and an N-TFT area 140, at the left and the right hand side, respectively, of FIG. 11(A).

On the resulting structure was deposited a silicon oxide film as a gate insulating film 153 to a thickness of from 500 to 2,000 Å, e.g., to a thickness of 700 Å. The conditions for the film depositlon were the same as those employed in depositing the silicon oxide film 151 which gave a blocking layer. Further, a small amount of fluorine may be added during the film deposition to fix sodium ions. In this EXAMPLE, a silicon nitride film 154 was deposited on the gate insulating film as a blocking layer to avoid reaction of the gate insulating film and the gate electrode to be formed thereon. This silicon nitride film had a thickness of from 50 to 200 Å, more specifically, 100 Å.

Further on the structure thus obtained above was deposited an aluminum film as a gate electrode material at a thickness of from 3,000 Å to 1.5 µm, 1 µm for example, by a known sputtering process.

Other useful materials for the gate electrode include molybdenum (Mo), tungsten (W), titanium (Ti), tantalum (Ta), and alloys thereof with silicon, as well as laminate wires of silicon with other metal films.

The use of a metal as the gate electrode, particularly, aluminum or a like material having a low resistance as in the present EXAMPLE, avoids gate delay (delay in the pulsed voltage which is transferred through the gate wire and distortion of the waveform) which becomes more pronounced with increasing area and finer patterning of the substrate, and hence facilitates fabrication of devices with a large-area substrate.

The aluminum film thus deposited was patterned through a second photomask ⑫ to obtain a structure as shown in FIG. 11(B), having a gate electrode 155 for the P-TFT and a gate electrode 156 for the N-TFT. Both of the gate electrodes were connected to a common gate wire 157.

The substrate was immersed into an AGW electrolyte having prepared by adding 9 parts of propylene glycol to 1 part of an aqueous 3% tartaric acid solution. A direct current (D.C.) was applied to the substrate by connecting the aluminum gate to the anode of a power source and using a platinum cathode as the counter electrode. The gate electrodes were each connected to

the respective gate wires, and a connection terminal was provided at the vicinity of the substrate end to clamp all the gate wires therewith for the connection. The anodic oxidation was conducted in this manner to form anodically oxidized films 158 and 159 around the gate electrodes as is shown in FIG. 11 (C).

In the anodic oxidation process, the electric current was applied first at a constant current density of 4 mA/cm$^2$ for 20 minutes, and then at a constant voltage for 15 minutes, to thereby obtain a 2,500 Å thick aluminum oxide film around the gate electrode. It is preferred to form the anodic oxide film as thick as possible, and this approach was taken in the present EXAMPLE as far as the process conditions permit.

As is shown in FIG. 11(D), the nitride film 154 and the silicon oxide film 153 on the semiconductor was removed by etching. Then, boron was doped over the whole substrate as an impurity for P-TFT, at a dose of from 1 x $10^{15}$ to 5 x $10^{15}$cm$^{-2}$ by ion implantation. The concentration of the doping was controlled to about $10^{19}$ atoms·cm$^{-3}$ to establish a source 160 and a drain 161 for the P-TFT. In the present EXAMPLE, the ion doping was conducted after removing the insulator films on the surface. However, it is also possible to conduct the doping through the insulator films 153 and 154, by changing the conditions of ion implantation.

Similarly, as shown in FIG. 11(E), a photoresist 464 was formed using a third photomask ⑬ to cover the P-TFT area, and phosphorus was doped by ion implantation to establish a source 162 and a drain 163 for the N-TFT. The phosphorus was added at a dose of from 1 x $10^{15}$ to 5 x $10^{15}$cm$^{-2}$, so that the doping concentration became about $10^{20}$ atoms·cm$^{-3}$. In this case, an oblique doping was used, in which the ion was bombarded obliquely to the substrate in such a manner that the direction of the ion beam may make an acute angle with respect to the surface of the substrate. This process allows the impurity ions to intrude into a lower portion under the anodic oxide film around the gate. In this manner, the ends of the source and the drain areas were roughly adjusted to match the end of the gate electrode. Thus, the anodically oxidized film can function sufficiently as an insulator to the contact wiring to be formed in the later steps, and hence excludes a step of forming an insulator film.

The structure was then re-heated at 600°C for a duration of 10 to 50 hours for annealing. Thus, the doped impurities in the source 160 and the drain 161 of the P-TFT, as well as those in the source 162 and the drain 163 of the N-TFT were activated to give P$^+$ and N$^+$. Under the gate electrodes 155 and 156 were formed channel forming regions 164 and 165. Instead of employing thermal annealing for the activation as in the present EXAMPLE, a laser beam may be irradiated to the source and the drain regions for the activation. In such a case, the activation can be performed in an instant and therefore the problem of thermal diffusion of the gate metal need not be considered. Accordingly, it is possible to omit the formation of silicon nitride film 154 which functions as a blocking layer on the gate insulating film.

A silicon oxide film as an insulator film was then deposited on the surface of the resulting structure by sputtering as mentioned above. The film is preferably as thick as possible, e. g., in a range of from 0.5 to 2.0 μm, 1.2 μm in this EXAMPLE. The film is then subjected to anisotropic etching from the upper side thereof to form a remainder area 166 at the vicinity of the side walls of a protrusion composed of the gate accompanied by the anodically oxidized film. The resulting structure is given in FIG. 11(F).

Then, the unnecessary portions were removed from the semiconductor film 152 by etching, using the protrusion above and the remainder area 166 as the mask. Then, the remainder area 166 around the protrusion was removed. Thus were obtained exposed semiconductor portions 152 at the outer side of the protrusion so that they may become a source and a drain region for each of the TFTs. The resulting structure is given in FIG. 11(G).

The whole structure was then covered with aluminum by sputtering, and after patterning the aluminum film through a fourth mask ⑭ to obtain leads 167 and 168 and contact portions 169 and 170, the unnecessary semiconductor film sticking out was removed by etching from the contacts 167, 168, 169, and 170; the gate electrodes 155 and 156; and the anodic oxide films 158 and 159 which accompany the gate electrodes. Thus were the elements separated from each other to complete a TFT. It can be seen from the foregoing description that a C/TFT pair was fabricated using merely four masks. The C/TFT pair thus obtained is shown in FIG. 11(H).

The TFT thus obtained comprises a gate electrode completely covered with an anodically oxidized film, and all the parts, exclusive of the source and the drain regions having contact connections sticking out from the gate portion, are established under the gate. The source and the drain electrodes are in contact with the source and the drain regions at two points, i.e., at the upper surface and the side face, to assure a sufficient ohmic contact.

Thus, as described in the foregoing, a C/TFT can be fabricated without heating the structure to a temperature 700°C or higher through the whole process. Thus, an economically advantageous substrate can be used instead of an expensive one such as of quartz, and hence the process is best suited for producing liquid crystal electro-optical devices of many pixels.

The thermal annealing was conducted twice in the present EXAMPLE, as shown in FIGS. 11(A) and 11(E). However, the annealing corresponding to that of FIG. 11 (A) may be omitted depending on the required device characteristics, and the thermal annealing may be integrated into one corresponding to that of FIG. 11(E) to speed up the process. Furthermore, the silicon nitride film 154 provided under the aluminum gate efficiently avoided reaction of the aluminum gate with the gate in-

sulating film under the gate, and a favorable interfacial characteristic was realized.

Then, an ITO film was deposited by sputtering between two TFTs, so that the output contact thereof may be connected to a liquid crystal device, through one of the pixel electrodes provided as a transparent electrode in a complementary structure. The ITO film was deposited in the temperature range of from room temperature to 150°C, which was annealed at 200 to 400°C in oxygen or in the atmosphere. The ITO film thus obtained was etched through a fifth photomask ⑮ to provide a pixel electrode 171. The resulting structure comprised a glass substrate having provided thereon a P-TFT 130, an N-TFT 140, and a transparent electrode 171 made from a transparent conductive film. The TFT thus obtained comprises a P-TFT having a mobility of 20 $cm^2$/Vsec with a $V_{th}$ of -5.9 V, and an N-TFT having a mobility of 40 $cm^2$/Vsec with a $V_{th}$ of +5.0 V.

In FIG. 12 is given the arrangement of the electrodes and the like of this liquid crystal electro-optical device. The cross sectional view along the line C-C' in FIG. 12 corresponds to those given in FIG. 11. The P-TFT 130 is provided to the crossing point of a first signal wire 172 and a third signal wire 157. Similarly, a P-TFT for another pixel is provided to the crossing point of the first signal wire 172 and another third signal wire 176 established as a right side neighbor of the wire 157. The N-TFT, on the other hand, is provided to the crossing point of a second signal wire 173 and the third signal wire 157. Furthermore, a P-TFT for another pixel is provided to the crossing point of another first signal wire 174 neighboring on the wire 172 and a third signal wire 157. Thus was obtained a matrix structure constructed from C/TFTs. The P-TFT 130 is connected to the first signal wire 172 through the contact of the drain 161, and the gate 155 is connected to the signal wire 157. The output terminal of the source 160 is connected to the pixel electrode 171 through a contact.

Similarly, the N-TFT 140 is connected to the second signal wire 173 through the contact of the source 162, to the signal wire 157 through the gate 156, and to the same pixel electrode 171 as in the case of P-TFT, by the output terminal of the drain 163 through a contact. Another C/TFT, which is provided next to the one described above and connected to the same third signal wire above, comprises a P-TFT 131 connected to the first signal wire 174 and an N-TFT 141 connected to a second signal wire 175. In this manner a pixel 180 is constructed inside a pair of signal wires 172 and 173, comprising a pixel electrode 171 composed of a transparent conductive film and a C/TFT pair. By repeating this structure along the vertical and horizontal directions, a 2 x 2 matrix can be extended into liquid crystal electro-optical devices having many pixels, such as those composed of 640 x 480 pixels and 1280 x 960 pixels. In the foregoing description, the impurity doped regions of the TFTs are referred to as source and drain for making the explanation simple. In the actual drive of the TFTs, the functions of those regions may differ in some cases.

In the TFT of the present EXAMPLE, the elements in each of the TFTs are separated into islands by removing the semiconductor film 152 through an etching process using a first photomask. Accordingly, the gate wiring outside the TFT areas is free of the underlying semiconductor film, and is established on the substrate or an insulator film having formed on the substrate. This structure avoids formation of a capacitance at the gate input side, and allows a high speed response.

A liquid crystal electro-optical device was then fabricated using the thus obtained substrate having established thereon the active elements. The substrate was first screen-coated with a UV-curable epoxy-modified acrylic resin having dispersed therein 50 % by weight of a nematic liquid crystal. In the process, a 125 mesh/inch screen was used for the coating, and a squeegee pressure of 1.5 kg/$cm^2$ was applied. The resulting emulsion thickness was 15 μm. After leveling for 10 minutes, the resin emulsion layer was cured with a high pressure mercury vapor lamp emitting a light having the main peak at a wavelength of 236 nm at an energy of 1,000 mJ. Thus was obtained a 12 μm thick light influencing layer.

A second electrode was then established on the cured resin layer by depositing thereon a 2,500 Å thick molybdenum (Mo) film by D.C. sputtering.

A black-colored epoxy resin was then applied to the surface by screen-printing, which was pre-baked at 50°C for 30 minutes and then baked at 180°C for 30 minutes to establish a 50 μm thick protective film.

A reflection-type liquid crystal display device was completed by connecting a TAB-shaped driver IC to the lead on the substrate. This device was comprises only one substrate.

In the EXAMPLE described above, a pair of TFTs in a complementary arrangement was provided as an active element to each of the pixels. However, the liquid crystal electro-optical devices are not limited to this structure, and plural pairs of TFTs in a complementary arrangement may be provided to each of the pixels. Otherwise, plural pairs of TFTs in a complementary arrangement may be provided to pixel contacts divided into plural contacts.

A liquid crystal electro-optical device comprising a dispersion type liquid crystal equipped with active elements was completed in this manner. Since the dispersion-type liquid crystal of the present EXAMPLE can be constructed on only one substrate, a light-weight and thin liquid crystal electro-optical device can be realized economically. More advantageously, a liquid crystal electro-optical device of high illuminance was obtained, because the device is constructed from a single substrate free of polarizer sheets and orientation control films.

EXAMPLE 3

Referring to FIG. 13, an example of a liquid crystal electro-optical device comprising pixels having provided to each thereof modified transfer-gate TFTs in a complementary arrangement is described. The TFTs in this EXAMPLE are fabricated basically in the same process as those in EXAMPLE 2, and the process steps proceed in a similar manner as shown in FIG. 11. The only difference is the arrangement of the C/TFT shown in FIG. 11, because the one used in the present EXAMPLE is a modified transfer-gate C/TFT. The actual arrangement and connection of the C/TFT of the present EXAMPLE is given in FIG. 14.

As shown in FIG. 13, a common gate wire 191 is connected with gates of a P-TFT 195 and a N-TFT 196. These TFTs are connected to another signal wire 193 through source and drain areas, and the other source and drain areas are connected to a common pixel electrode.

The fabrication process proceeds the same to FIG. 11(G). The structure obtained to the step shown in FIG. 11(G) is coated with a silicon nitride film 200 at a thickness of from 500 to 2,000 Å. The resulting silicon nitride film 200 is anisotropically etched along the direction vertical to the substrate to remain the silicon nitride film on the side wall of the anodically oxidized film 201 provided on the gate electrode. The silicon nitride film need not be left out uniformly, provided that the film remains at least on the gate 207 and on the gate insulating film at the proximity of the semiconductor. This silicon nitride film 200 functions as a protective layer to avoid short circuit at the vicinity of the end portion of a gate insulating film 203, caused by a metallic wiring 202, a source area 204, and a drain area 205, upon formation of source and drain 202 at the later steps.

On the surface of the resulting structure is then deposited an interlayer insulator film and a silicon oxide film 206 at a thickness of from 1,000 Å to 2 μm, e.g., 6,000 Å in this case. After forming a photoresist thereon, a mask is formed on the gate 207 using the gate as the mask by exposure to light from the substrate side. Then an interlayer insulator film 206 can be obtained on the gate by etching.

The process is then forwarded in the same manner as in FIGS. 11(H) and 11(I), to thereby complete the structure into a modified transfer-gate TFT having an arrangement and structure as shown in FIGS. 14(A), 14 (B), and 14(C). In FIGS. 14(B) and 14(C) are shown clearly that the gate 207 always comprises thereon an interlayer insulator film 206, by which an effective interlayer insulating function is provided to the crossings of the lead portion of the gate wiring 207 with the lead portion of the source and drain wiring 202. Thus, as is shown in FIG. 14(A), the formation of unfavorable wiring capacitance could be avoided.

As was described above, an active element substrate was obtained with the same number of masks as that in EXAMPLE 2, yet having reduced in capacitance around the wiring and composed of TFTs having such a structure less apt to cause short circuit at the vicinity of the gate insulating film.

An active matrix super-twisted nematic (STN) liquid crystal electro-optical device was then produced, by combining and adhering the substrate obtained above as a first substrate with a second substrate having subjected to orientation treatment and having provided thereon a counter electrode, and injecting an STN liquid crystal therebetween, according to a known technology.

In the foregoing EXAMPLES, the TFTs embodying the present invention were applied to liquid crystal electro-optical devices.

However, the EXAMPLES above are not limiting, and the TFTs can be readily applied to other devices and three-dimensional IC elements and the like.

The present invention enables fabrication of TFT elements using considerably reduced number of masks. Accordingly, semiconductor devices can be produced through a far simpler fabrication process and with increased production yield by applying the TFTs of this structure to the fabrication of the devices. Thus, the present invention provides semiconductor devices at a reduced production cost.

The TFT embodying the present invention comprises a metallic gate electrode having subjected to anodic oxidation to form an oxide film on the surface thereof, so that a wiring comprising a three-dimensional crossing can be established thereon. Furthermore, the feeding points of the source and the drain are provided very near to the channel by the use of said gate with an oxide film around it, and by exposing only the contact portions of the source and the drain out of the gate. Thus were avoided the drop of frequency characteristics of the device and the increase of ON resistivity.

Furthermore, in an embodiment according to the present invention in which an aluminum gate is used, hydrogen having incorporated into the gate oxide film could be reduced during the annealing step by dissociating $H_2$ into H taking advantage of the catalytic effect of aluminum. Thus, the interfacial density of states ($Q_{SS}$) could be lowered as compared to the case in which a silicon gate is used, and, by this effect, an element having improved characteristics was realized.

The source and the drain of the TFTs embodying the present invention were established in a self-aligned manner. The same was done in the positioning of contact portions of the source and the drain. Thus, the area necessary to accommodate the elements to construct a TFT was reduced, and hence was effective for achieving a higher degree of integration. In the case the TFTs were used as active elements for a liquid crystal electrooptical device, the aperture ratio of the liquid crystal panel was increased.

The anodically oxidized film around the gate was taken full advantage of, and a TFT having a distinguished structure was proposed. This TFT, moreover,

can be fabricated with minimized number of masks, the minimum being 2 masks.

In a C/TFT embodying the present invention, a semi-amorphous or semi-crystalline semiconductor was used. However, the semiconductor may be replaced by semiconductors differing in crystal structure if possible, provided that they are used for the same purpose. By the use of a self-aligned C/TFT, a rapid processing was possible. However, this is not limiting, and TFTs may be fabricated by a non-self-aligned manner without using ion implantation. Furthermore, it should be noted that the present invention is not limited only to stagger-type TFTs, but also encompasses inverted-type stagger TFTs and other types of TFTs.

Having thus described the invention by reference to particular embodiments, it is to be appreciated that the described embodiments are exemplary only and are susceptible to modification and variation without departure from the scope of the invention as set forth in the appended claims.

**Claims**

1. A method of manufacturing a semiconductor device comprising:

   forming a semiconductor layer (2,23,102,130) on an insulating surface (1,101,151);
   forming a gate insulating layer (6,27,106,153) on said semiconductor layer (2,23,102,130);
   forming a metal gate electrode (8,25,108,155) on said gate insulating layer (6,27,106,153);
   anodic oxidizing side surfaces of said gate electrode to form an anodic oxide layer (10,40,110,155) comprising said gate metal thereon; and
   introducing dopant impurities into portions (3,33,35,103,161,162) of said semiconductor layer (2,23,102,130) in a self-aligned manner with respect to said gate electrode and said oxide layer (10,40,110,158), thereby forming source and drain impurity doped regions (3,33,35,103,161,162) in said semiconductor layer and a channel region (34) therebetween;
   wherein the formation of said oxide layer (10,40,110,158) provides offset regions in said channel region (34) adjacent said oxide layer,
   characterised in that said step of anodic oxidizing includes anodic oxidizing upper surfaces of said gate electrode and in that, said method further comprises controlling the size of said offset regions by controlling the thickness of said oxide layer.

2. The method of claim 1 further comprising:

   forming an insulating film (41) on said surface (1) over said gate electrode (25); and
   forming at least one contact hole (42) over one of said source and drain regions (33,35) in said insulating film (41) with a side surface of said contact hole (42) located substantially on a side surface of said oxide layer (40).

3. The method of claim 2 wherein said contact hole forming step is carried out with said gate electrode (25) and said oxide layer (40) as a mask.

4. The method of claim 2 wherein said contact hole forming step is carried out to leave the insulating film (41) on an upper surface of said gate electrode (25) by use of a photomask (31).

5. The method of claim 4 wherein the insulating film (41) is left on said upper surface of said gate electrode (25) with said oxide layer (40) extending therebetween by said contact hole forming step.

6. The method of any preceding claim wherein said semiconductor layer forming step is carried out by forming a silicon semiconductor layer (23) containing hydrogen therein on said surface (1) and subsequently crystallizing said silicon semiconductor layer (23) by thermal treatment.

7. The method of claim 1 further comprising:

   forming an insulating film (112) on said gate insulating layer (6,106) over said gate electrode (8,108);
   selectively removing the insulating film (112) and the gate insulating layer (6,106) by anisotropic etching to leave a portion (113) of the insulating film (112) and the gate insulating layer (6,106) around a side of said gate electrode (8,108);
   selectively removing the semiconductor layer (2,102) by etching with said gate electrode (8,108), said oxide layer (10,110) and the remaining portion (113) of the insulating film (112) as a mask;
   exposing a portion (103) of the semiconductor layer (2,102) provided under the remaining portion (113) of the insulating film (112) by removing the remaining portion of the insulating film and a portion of the gate insulating layer (6,106) provided under the remaining portion (113) of the insulating film (112) by etching;
   forming a conductive layer (7,107) on said surface (1,101) over said oxide layer (10,110) and the exposed portion (103) of the semiconductor layer (2,102); and
   patterning said conductive layer (7,107) with a mask to form source and drain electrodes (7,107) which extend on said oxide layer

(10,110) and are in contact with upper and side surfaces of the exposed portion (103) of the semiconductor layer (2,102).

8. The method of claim 7 wherein said step of introducing dopant impurities comprises implanting impurities into exposed portions (103) of the semiconductor layer (2,102) to form said source and drain regions (3,33,35,103,161,162) therein.

9. The method of claim 7 wherein said step of introducing dopant impurities comprises implanting impurities into the semiconductor layer (2,102) with said oxide layer (10,110) as a mask before said insulating film forming step.

10. The method of claim 1 wherein said step of forming a semiconductor layer (2,102) comprises forming a semiconductor island (130) on said surface (151) and said method further comprises:

selectively removing the gate insulating layer (153) with said gate electrode (155) and said oxide layer (158) as a mask;
forming an insulating film on said surface (151) over said oxide layer (158);
selectively removing the insulating film by anisotropic etching to leave a remaining portion (166) of the insulating film around a side of said gate electrode (155);
selectively removing the semiconductor island (130) by etching with said gate electrode (155), said oxide layer (158) and the remaining portion (166) of the insulating film as a mask;
removing the remaining portion (166) of the insulating film by etching to expose a portion (160,161) of the semiconductor island (130) provided under the remaining portion (166) of the insulating film;
forming a conductive layer (167,168) on said surface (151) over the exposed portion (160,161) of the semiconductor island (130); and
patterning said conductive layer with a mask to form source and drain electrodes (167,168) which extend on said oxide layer (158) and are in contact with the exposed portion (160,161) of the semiconductor island (130).

11. The method of any preceding claim, wherein said step of forming a gate electrode (8,25,108,155) comprises forming a metal alloy gate electrode or a metal/silicon laminate wire gate electrode.

12. The method of any preceding claim, wherein the formation of said oxide layer (10,40,110,158) is controlled to provide an oxide layer having a thickness in the range 10nm to 50nm.

13. The method of any preceding claim, further comprising forming a buffer layer (154) between said gate insulating layer (6,27,106,153) and said metal gate electrode (8,25,108,155).

14. A semiconductor device comprising:

a semiconductor layer (2,23,102,130) on an insulating surface (1,101,151), said semiconductor layer (2,23,102,130) comprising source and drain impurity doped regions (3,33,35,103,161,162) and a channel region (34) therebetween;
a gate insulating layer (6,27,106,153) on said semiconductor layer (2,23,102,130),
a metal gate electrode (8, 25, 108, 155) on said gate insulating layer (6,27,106,153) adjacent to said channel region;
an anodic oxide layer (10,40,110,158) comprising said gate metal formed on side surfaces of said gate electrode (8,25,108,155);
wherein said channel region (34) includes offset regions adjacent said anodic oxide layer (10,40,110,158) the size of said offset regions being determined by the thickness of said oxide layer characterised in that said anodic oxide layer is also formed on upper surfaces of said gate electrode.

15. The semiconductor device of claim 14 wherein said device further comprises source and drain electrodes (7,43,52,53) connected to said source and drain regions (3,33,35,103,161,162) respectively.

16. The semiconductor device of claim 15 wherein a side of at least one of said source and drain electrodes (7,43,52,53) is substantially aligned with a side of said oxide layer (10,40,110,158).

17. The semiconductor device of claim 16 wherein sides of both of said source and drain electrodes (7,43,52,53) are substantially aligned with sides of said oxide layer (10,40,110,158).

18. The semiconductor device of any of claims 15 to 17 wherein said oxide layer (10,40,110,158) is in contact with said gate electrode (8,25,108,155) and said at least one of said source and drain electrodes (7,43,52,53).

19. The semiconductor device of any of claims 14 to 18 wherein a side of one of said source and drain regions (3,33,35,103,161,162) is aligned with a side of said oxide layer (10,40,110,158).

20. The semiconductor device of any of claims 14 to 19 wherein said gate electrode (8,25,108,155) is distant from one of said source and drain regions

(3,33,35,103,161,162) substantially by a thickness of said oxide layer (10,40,110,158) in a direction from one of said source and drain regions to the other of said source and drain regions.

21. The semiconductor device of claim 15 or any claim dependent thereon wherein said source and drain electrodes (7,43,52,53) extend on said upper surface of said oxide layer (10,40,110,158).

22. The semiconductor device of claim 15 or any claim dependent thereon wherein said semiconductor layer (2,23,102,130) is provided on a substrate (1,150), said source and drain electrodes (7,43,52,53) are provided on said substrate and side surfaces of said source and drain regions (3,33,35,103,161,162) are side surfaces of said semiconductor layer.

23. The semiconductor device of any of claims 14 to 22, wherein said gate electrode (8,25,108,155) comprises a metal alloy or a metal/silicon laminate wire.

24. The semiconductor device of any of claims 14 to 23, wherein the thickness of said oxide layer is in the range of 10nm to 50nm.

25. The semiconductor device of any of claims 14 to 24, further comprising a buffer layer (154) formed between the gate electrode (8,25,108,155) and the gate insulating layer (6,27,106,153).

26. An electro-optical device incorporating one or more devices as claimed in any of claims 14 to 25.

**Patentansprüche**

1. Verfahren zur Herstellung einer Halbleitervorrichtung, aufweisend:

   Ausbilden einer Halbleiterschicht (2, 23, 102, 130) auf einer isolierenden Oberfläche (1, 101, 151),
   Ausbilden einer Gate-Isolierschicht (6, 27, 106, 153) auf der Halbleiterschicht (2, 23, 102, 130)
   Ausbilden einer Metall-Gate-Elektrode (8, 25, 108, 155) auf der Gate-Isolierschicht (6, 27, 106, 153),
   anodische Oxidation von Seitenflächen der Gate-Elektrode zur Ausbildung einer Anodenoxidschicht (10, 40, 110, 155), die das darauf befindliche Gate-Metall beinhaltet, und
   Einführen dotierender Störstoffe in Abschnitte (3, 33, 35, 103, 161, 162) der Halbleiterschicht (2, 23, 102, 130) nach selbstausrichtender Art bezüglich der Gate-Elektrode und der Oxidschicht (10, 40, 110, 158), um in der Halbleiterschicht störstoffdotierte Source- und Drain-Bereiche (3, 33, 35, 103, 161, 162) und zwischen diesen einen Kanalbereich (34) zu bilden,
   wobei die Ausbildung der Oxidschicht (10, 40, 110, 158) in dem Kanalbereich (34), bei der Oxidschicht Versatzbereiche liefert,

   dadurch **gekennzeichnet**, daß der Schritt der anodischen Oxidation eine anodische Oxidation von oberen Oberflächen der Gate-Elektrode beinhaltet und die Größe der Versatzbereiche durch Steuerung der Dicke der Oxidschicht gesteuert wird.

2. Verfahren nach Anspruch 1, aufweisend:

   Ausbilden eines Isolierfilms (41) auf der genannten Oberfläche (1) über der Gate-Elektrode (25), und
   Ausbilden mindestens eines Kontaktlochs (42) in dem Isolierfilm (41) über dem Source- oder dem Drain-Bereich (33, 35), wobei eine Seitenfläche des Kontaktlochs (42) im wesentlichen auf einer Seitenfläche der Oxidschicht (40) liegt.

3. Verfahren nach Anspruch 2, wobei der Schritt zur Ausbildung des Kontaktlochs mit der Gate-Elektrode (25) und der Oxidschicht (40) als Maske durchgeführt wird.

4. Verfahren nach Anspruch 2, wobei der Schritt zur Ausbildung des Kontaktlochs unter Belassung des Isolierfilms (41) auf einer oberen Oberfläche der Gate-Elektrode (25) durchgeführt wird, indem eine Photomaske (31) verwendet wird.

5. Verfahren nach Anspruch 4, wobei der Isolierfilm (41) bei dem Schritt zur Ausbildung des Kontaktlochs auf der oberen Oberfläche der Gate-Elektrode (25) belassen wird und die Oxidschicht (40) zwischen diesen verläuft.

6. Verfahren nach einem der vorhergehenden Ansprüche, wobei der Schritt zur Ausbildung der Halbleiterschicht durch Ausbilden einer Wasserstoff enthaltenden Silizium-Halbleiterschicht (23) auf der Oberfläche (1) und nachfolgendes Kristallisieren der Silizium-Halbleiterschicht (23) mittels einer Wärmebehandlung durchgeführt wird.

7. Verfahren nach Anspruch 1, aufweisend:

   Ausbilden eines Isolierfilms (112) auf der Gate-Isolierschicht (6, 106) über der Gate-Elektrode (8, 108),
   ausgewähltes Entfernen des Isolierfilms (112) und der Gate-Isolierschicht (6, 106) mittels an-

isotropen Ätzens unter Belassung eines Abschnitts (113) des Isolierfilms (112) und der Gate-Isolierschicht (6, 106) um eine Seite der Gate-Elektrode (8, 108),
ausgewähltes Entfernen der Halbleiterschicht (2, 102) durch Ätzen mit der Gate-Elektrode (8, 108), der Oxidschicht (10, 110) und des verbliebenen Abschnitts (113) des Isolierfilms (112) als Maske,
Freilegen eines Abschnitts (103) der Halbleiterschicht (2, 102) unter dem verbliebenen Abschnitt (113) des Isolierfilms (112), indem der verbliebene Abschnitt des Isolierfilms und ein Abschnitt der Gate-Isolierschicht (6, 106) unter dem verbliebenen Abschnitt (113) des Isolierfilms (112) durch Ätzen entfernt werden,
Ausbilden einer leitfähigen Schicht (7, 107) auf der genannten Oberfläche (1, 101) über der Oxidschicht (10, 110) und dem freigelegten Abschnitt (103) der Halbleiterschicht (2, 102), und
Strukturieren der leitfähigen Schicht (7, 107) mittels einer Maske, um Source- und Drain-Elektroden (7, 107) auszubilden, die auf der Oxidschicht (10, 110) verlaufen und sich in Kontakt mit der oberen Fläche und den Seitenflächen des freigelegten Abschnitts (103) der Halbleiterschicht (2, 102) befinden.

8. Verfahren nach Anspruch 7, wobei der Schritt zur Einführung dotierender Störstoffe das Implantieren von Störstoffen in freigelegte Abschnitte (103) der Halbleiterschicht (2, 102) beinhaltet, um darin die genannten Source- und Drain-Bereiche (3, 33, 35, 103, 161, 162) auszubilden.

9. Verfahren nach Anspruch 7, wobei der Schritt zur Einführung dotierender Störstoffe das Implantieren von Störstoffen in die Halbleiterschicht (2, 102) unter Verwendung der Oxidschicht (10, 110) als Maske vor dem Schritt zur Ausbildung des Isolierfilms umfaßt.

10. Verfahren nach Anspruch 1, wobei der Schritt des Ausbildens einer Halbleiterschicht (2, 102) das Ausbilden einer Halbleiterinsel (130) auf der genannten Oberfläche (151) beinhaltet und das Verfahren außerdem aufweist:

ausgewähltes Entfernen der Gate-Isolierschicht (153) mittels der Gate-Elektrode (155) und der Oxidschicht (158) als Maske,
Ausbilden eines Isolierfilms auf der genannten Oberfläche (151) über der Oxidschicht (158),
ausgewähltes Entfernen des Isolierfilms durch anisotropes Ätzen unter Belassung eines verbleibenden Abschnitts (166) des Isolierfilms um eine Seite der Gate- Elektrode (155),
ausgewähltes Entfernen der Halbleiterinsel (130) durch Ätzen mittels der Gate-Elektrode (155), der Oxidschicht (158) und des verbliebenen Abschnitts (166) des Isolierfilms als Maske,
Entfernen des verbliebenen Abschnitts (166) des Isolierfilms durch Ätzen, um einen Abschnitt (160, 161) der Halbleiterinsel (130) unter dem verbliebenen Abschnitt (166) des Isolierfilms freizulegen,
Ausbilden einer leitfähigen Schicht (167, 168) auf der Oberfläche (151) über dem freigelegten Abschnitt (160, 161) der Halbleiterinsel (130), und
Strukturieren der leitfähigen Schicht mittels einer Maske, um Source- und Drain-Elektroden (167, 168) zu bilden, die auf der Oxidschicht (158) verlaufen und sich in Kontakt mit dem freigelegten Abschnitt (160, 161) der Halbleiterinsel (130) befinden.

11. Verfahren nach einem der vorhergehenden Ansprüche, wobei der Schritt zur Ausbildung einer Gate-Elektrode (8, 25, 108, 155) die Ausbildung einer Metallegierungs-Gate-Elektrode oder einer Metall/Silizium-Laminatleitungs-Gate-Elektrode beinhaltet.

12. Verfahren nach einem der vorhergehenden Ansprüche, wobei die Ausbildung der Oxidschicht (10, 40, 110, 158) so gesteuert wird, daß eine Oxidschicht einer Dicke im Bereich von 10nm bis 50nm vorgesehen wird.

13. Verfahren nach einem der vorhergehenden Ansprüche, mit dem Ausbilden einer Pufferschicht (154) zwischen der Gate-Isolierschicht (6, 27, 106, 153) und der Metall-Gate-Elektrode (8, 25, 108, 155).

14. Halbleitervorrichtung, aufweisend:

eine Halbleiterschicht (2, 23, 102, 130) auf einer Isolierfläche (1, 101, 151), wobei die Halbleiterschicht (2, 23, 102, 130) störstoffdotierte Source- und Drain-Bereiche (3, 33, 35, 103, 161, 162) sowie einen Kanalbereich (34) zwischen diesen aufweist,
eine Gate-Isolierschicht (6, 27, 106, 153) auf der Halbleiterschicht (2, 23, 102, 130),
eine Metall-Gate-Elektrode (8, 25, 108, 155) auf der Gate-Isolierschicht (6, 27, 106, 153) bei dem Kanalbereich,
eine Anodenoxidschicht (10, 40, 110, 158) mit dem genannten Gate-Metall, ausgebildet auf Seitenflächen der Gate-Elektrode (8, 25, 108, 155),
wobei der genannte Kanalbereich (34) bei der Anodenoxidschicht (10, 40, 110, 158) Versatzereiche beinhaltet, deren Größe von der Dicke

der Oxidschicht bestimmt ist,

dadurch **gekennzeichnet**, daß die Anodenoxidschicht auch auf oberen Oberflächen der Gate-Elektrode ausgebildet ist.

15. Vorrichtung nach Anspruch 14, mit Source- und Drain Elektroden (7, 43, 52, 53), die entsprechenderweise mit den Source- und Drain-Bereichen (3, 33, 35, 103, 161, 162) verbunden sind.

16. Vorrichtung nach Anspruch 15, wobei eine Seite mindestens einer der Source- und Drain-Elektroden (7, 43, 52, 53) im wesentlichen zu einer Seite der Oxidschicht (10, 40, 110, 158) ausgerichtet ist.

17. Vorrichtung nach Anspruch 16, wobei die Seiten sowohl der Source- als auch der Drain Elektrode (7, 43, 52, 53) im wesentlichen zu den Seiten der Oxidschicht (10, 40, 110, 158) ausgerichtet sind.

18. Vorrichtung nach einem der Ansprüche 15 bis 17, wobei sich die Oxidschicht (10, 40, 110, 158) in Kontakt mit der Gate-Elektrode (8, 25, 108, 155) und der genannten mindestens einen der Source- und Drain-Elektroden (7, 43, 52, 53) befindet.

19. Vorrichtung nach einem der Ansprüche 14 bis 18, wobei eine Seite eines der Source- und Drain-Bereiche (3, 33, 35, 103, 161, 162) zu einer Seite der Oxidschicht (10, 40, 110, 158) ausgerichtet ist.

20. Vorrichtung nach einem der Ansprüche 14 bis 19, wobei die Gate-Elektrode (8, 25, 108, 155) von einem der Source-und Drain-Bereiche (3, 33, 35, 103, 161, 162) im wesentlichen die Dicke der Oxidschicht (10, 40, 110, 158) in Richtung von einem zum anderen der Source- und Drain-Bereiche als Abstand aufweist.

21. Vorrichtung nach Anspruch 15 oder einem der davon abhängigen Ansprüche, wobei die Source- und Drain-Elektroden (7, 43, 52, 53) im wesentlichen auf der oberen Oberfläche der Oxidschicht (10, 40, 110, 158) verlaufen.

22. Vorrichtung nach Anspruch 15 oder einem der davon abhängigen Ansprüche, wobei die Oxidschicht (2, 23, 102, 130) auf einem Substrat (1, 150) vorgesehen ist, die Source- und die Drain-Elektrode (7, 43, 52, 53) auf dem Substrat vorgesehen sind und Seitenflächen der Source- und Drain-Bereiche (3, 33, 35, 103, 161, 162) Seitenflächen der Halbleiterschicht darstellen.

23. Vorrichtung nach einem der Ansprüche 14 bis 22, wobei die Gate-Elektrode (8, 25, 108, 155) eine Metallegierungsleitung oder eine Metall/Silizium-Laminatleitung beinhaltet.

24. Vorrichtung nach einem der Ansprüche 14 bis 23, wobei die Dicke der Oxidschicht im Bereich von 10nm bis 50nm liegt.

25. Vorrichtung nach einem der Ansprüche 14 bis 24, mit einer zwischen der Gate-Elektrode (8, 25, 108, 155) und der Gate-Isolierschicht (6, 27, 106, 153) ausgebildeten Pufferschicht (154).

26. Elektrooptische Vorrichtung mit einer oder mehreren Vorrichtungen nach einem der Ansprüche 14 bis 25.

**Revendications**

1. Procédé de fabrication d'un composant à semiconducteur comprenant :

   la formation d'une couche à semiconducteur (2, 23, 102, 130) sur une surface isolante (1, 101, 151) ;
   la formation d'une couche isolante de grille (6, 27, 106, 153) sur ladite couche à semiconducteur (2, 23, 102, 130) ;
   la formation d'une électrode de grille métallique (8, 25, 108, 155) sur ladite couche isolante de grille (6, 27, 106, 153) ;
   l'oxydation anodique des surfaces latérales de ladite électrode de grille pour former une couche d'oxyde anodique (10, 40, 110, 155) comprenant ledit métal de grille sur cette dernière ; et
   l'introduction d'impuretés de dopage dans des parties (3, 33, 35, 103, 161, 162) de ladite couche à semiconducteur (2, 23, 102, 130) d'une manière auto-alignée par rapport à ladite électrode de grille et à ladite couche d'oxyde (10, 40, 110, 158), formant, de ce fait, des zones dopées en impuretés de source et de drain (3, 33, 35, 103, 161, 162) dans ladite couche à semiconducteur et dans une zone de canal (34) entre elles ;

   dans lequel la formation de ladite couche d'oxyde (10, 40, 110, 158) réalise des zones décalées dans ladite zone de canal (34) adjacente à ladite couche d'oxyde, caractérisé en ce que ladite étape d'oxydation anodique comprend l'oxydation anodique de surfaces supérieures de ladite électrode de grille et en ce que, ledit procédé comprend, de plus, la maîtrise de la taille desdites zones décalées en maîtrisant l'épaisseur de ladite couche d'oxyde.

2. Procédé selon la revendication 1, comprenant, de

plus :

la formation d'un film isolant (41) sur ladite surface (1) au-dessus de ladite électrode de grille (25) ; et
la formation d'au moins un trou de contact (42) au-dessus d'une desdites zones de source et de drain (33, 35) dans ledit film isolant (41) avec une surface latérale dudit trou de contact (42) située sensiblement sur une surface latérale de ladite couche d'oxyde (40).

3. Procédé selon la revendication 2, dans lequel ladite étape de formation de trou de contact est exécutée avec ladite électrode de grille (25) et ladite couche d'oxyde (40) en tant que masque.

4. Procédé selon la revendication 2, dans lequel ladite étape de formation de trou de contact est exécutée pour laisser le film isolant (41) sur une surface supérieure de ladite électrode de grille (25) par l'utilisation d'un masque de photogravure (31).

5. Procédé selon la revendication 4, dans lequel le film isolant (41) est laissé sur ladite surface supérieure de ladite électrode de grille (25), ladite couche d'oxyde (40) s'étendant entre elles par ladite étape de formation de trou de contact.

6. Procédé selon l'une quelconque des revendications précédentes, dans lequel ladite étape de formation de couche à semiconducteur est exécutée en formant une couche à semiconducteur de silicium (23) contenant de l'hydrogène en son sein sur ladite surface (1) et en cristallisant ensuite ladite couche à semiconducteur de silicium (23) par un traitement thermique.

7. Procédé selon la revendication 1, comprenant, de plus :

la formation d'un film isolant (112) sur ladite couche isolante de grille (6, 106) au-dessus de ladite électrode de grille (8, 108) ;
l'enlèvement, de manière sélective, du film isolant (112) et de la couche isolante de grille (6, 106) par une attaque anisotrope pour laisser une partie (113) du film isolant (112) et la couche isolante de grille (6, 106) autour d'un côté de ladite électrode de grille (8, 108) ;
l'enlèvement, de manière sélective, de la couche à semiconducteur (2, 102) par une attaque, ladite électrode de grille (8, 108), ladite couche d'oxyde (10, 110) et la partie restante (113) du film isolant (112) servant de masque ;
l'exposition d'une partie (103) de la couche à semiconducteur (2, 102) disposée sous la partie restante (113) du film isolant (112) en retirant la partie restante du film isolant et une partie de la couche isolante de grille (6, 106) disposée sous la partie restante (113) du film isolant (112) par attaque ;
la formation d'une couche conductrice (7,107) sur ladite surface (1, 101) au-dessus de ladite couche d'oxyde (10, 110) et de la partie exposée (103) de la couche à semiconducteur (2, 102) ; et
la formation de motifs de ladite couche conductrice (7, 107) avec un masque pour former des électrodes de source et de drain (7, 107) qui s'étendent sur ladite couche d'oxyde (10, 110) et qui sont en contact avec des surfaces supérieures et latérales de la partie exposée (103) de la couche à semiconducteur (2, 102).

8. Procédé selon la revendication 7, dans lequel ladite étape d'introduction d'impuretés de dopage comprend l'implantation d'impuretés dans des zones exposées (103) de la couche à semiconducteur (2, 102) pour former lesdites zones de source et de drain (3, 33, 35, 103, 161, 162) en son sein.

9. Procédé selon la revendication 7, dans lequel ladite étape d'introduction d'impuretés de dopage comprend l'implantation d'impuretés dans la couche à semiconducteur (2, 102), ladite couche d'oxyde (10, 110) servant de masque, avant ladite étape de formation de film isolant.

10. Procédé selon la revendication 1, dans lequel ladite étape de formation d'une couche à semiconducteur (2, 102) comprend la formation d'un îlot semiconducteur (130) sur ladite surface (151) et ledit procédé comprend, de plus :

l'enlèvement, de manière sélective, de la couche isolante de grille (153), ladite électrode de grille (155) et ladite couche d'oxyde (158) servant de masque ;
la formation d'un film isolant sur ladite surface (151) au-dessus de ladite couche d'oxyde (158) ;
l'enlèvement, de manière sélective, du film isolant par attaque anisotrope pour laisser une partie restante (166) du film isolant autour d'un côté de ladite électrode de grille (155) ;
l'enlèvement, de manière sélective, de l'îlot semiconducteur (130) par une attaque, ladite électrode de grille (155), ladite couche d'oxyde (158) et la partie restante (166) du film isolant servant de masque ;
l'enlèvement de la partie restante (166) du film isolant par une attaque pour exposer une partie (160, 161) de l'îlot semiconducteur (130) disposé sous la partie restante (166) du film isolant ;
la formation d'une couche conductrice (167,

168) sur ladite surface (151) au-dessus de la partie exposée (160, 161) de l'îlot semiconducteur (130) ; et
la formation de motifs de ladite couche conductrice avec un masque pour former des électrodes de source et de drain (167, 168) qui s'étendent sur ladite couche d'oxyde (158) et qui sont en contact avec la partie exposée (160, 161) de l'îlot semiconducteur (130).

**11.** Procédé selon l'une quelconque des revendications précédentes, dans lequel ladite étape de formation d'une électrode de grille (8, 25, 108, 155) comprend la formation d'une électrode de grille d'alliage métallique ou d'une électrode de grille à fil laminé de métal/silicium.

**12.** Procédé selon l'une quelconque des revendications précédentes, dans lequel la formation de ladite couche d'oxyde (10, 40, 110, 158) est commandée pour donner une couche d'oxyde ayant une épaisseur dans la plage de 10 nm à 50 nm.

**13.** Procédé selon l'une quelconque des revendications précédentes, comprenant, de plus, la formation d'une couche tampon (154) entre ladite couche isolante de grille (6, 27, 106, 153) et ladite électrode de grille métallique (8, 25, 108, 155).

**14.** Composant à semiconducteur, comprenant :

une couche à semiconducteur (2, 23, 102, 130) sur une surface isolante (1, 101, 151), ladite couche à semiconducteur (2, 23, 102, 130) comprenant des zones (3, 33, 35, 103, 161, 162) dopées en impuretés de source et de drain et une zone de canal (34) entre elles ;
une couche isolante de grille (6, 27, 106, 153) sur ladite couche à semiconducteur (2, 23, 102, 130),
une électrode de grille métallique (8, 25, 108, 155) sur ladite couche isolante de grille (6, 27, 106, 153) adjacente à ladite zone de canal ;
une couche d'oxyde anodique (10, 40, 110, 158) comprenant ledit métal de grille formé sur des surfaces latérales de ladite électrode de grille (8, 25, 108, 155) ;
dans lequel ladite zone de canal (34) comprend des zones décalées adjacentes à ladite couche d'oxyde anodique (10, 40, 110, 158), la taille desdites zones décalées étant déterminée par l'épaisseur de ladite couche d'oxyde, caractérisé en ce que ladite couche d'oxyde anodique est également formée sur des surfaces supérieures de ladite électrode de grille.

**15.** Composant à semiconducteur selon la revendication 14, dans lequel ledit composant comprend, de plus, des électrodes de source et de drain (7, 43, 52, 53) respectivement reliées auxdites zones de source et de drain (3, 33, 35, 103, 161, 162).

**16.** Composant à semiconducteur selon la revendication 15, dans lequel un côté d'au moins une desdites électrodes de source et de drain (7, 43, 52, 53) est sensiblement aligné avec un côté de ladite couche d'oxyde (10, 40, 110, 158).

**17.** Composant à semiconducteur selon la revendication 16, dans lequel des côtés des deux électrodes de source et de drain (7, 43, 52, 53) sont sensiblement alignés avec des côtés de ladite couche d'oxyde (10, 40, 110, 158).

**18.** Composant à semiconducteur selon l'une quelconque des revendications 15 à 17, dans lequel ladite couche d'oxyde (10, 40, 110, 158) est en contact avec ladite électrode de grille (8, 25, 108, 155) et ladite au moins une desdites électrodes de source et de drain (7, 43, 52, 53).

**19.** Composant à semiconducteur selon l'une quelconque des revendications 14 à 18, dans lequel un côté d'une des zones de source et de drain (3, 33, 35, 103, 161, 162) est aligné avec un côté de ladite couche d'oxyde (10, 40, 110, 158).

**20.** Composant à semiconducteur selon l'une quelconque des revendications 14 à 19, dans lequel ladite électrode de grille (8, 25, 108, 155) est distante depuis l'une desdites zones de source et de drain (3, 33, 35, 103, 161, 162) sensiblement d'une épaisseur de ladite couche d'oxyde (10, 40, 110, 158) dans un sens depuis l'une desdites zones de source et de drain jusqu'à l'autre desdites zones de source et de drain.

**21.** Composant à semiconducteur selon la revendication 15 ou selon l'une quelconque des revendications dépendantes de cette dernière, dans lequel lesdites électrodes de source et de drain (7, 43, 52, 53) s'étendent sur ladite surface supérieure de ladite couche d'oxyde (10, 40, 110, 158).

**22.** Composant à semiconducteur selon la revendication 15 ou selon l'une quelconque des revendications dépendantes de cette dernière, dans lequel ladite couche à semiconducteur (2, 23, 102, 130) est disposée sur un substrat (1, 150), lesdites électrodes de source et de drain (7, 43, 52, 53) sont disposées sur ledit substrat et des surfaces latérales desdites zones de source et de drain (3, 33, 35, 103, 161, 162) sont des surfaces latérales de ladite couche à semiconducteur.

**23.** Composant à semiconducteur selon l'une quelcon-

que des revendications 14 à 22, dans lequel ladite électrode de grille (8, 25, 108, 155) comprend un alliage métallique ou un fil laminé de métal/silicium.

**24.** Composant à semiconducteur selon l'une quelconque des revendications 14 à 23, dans lequel l'épaisseur de ladite couche d'oxyde est dans la plage de 10 nm à 50 nm.

**25.** Composant à semiconducteur selon l'une quelconque des revendications 14 à 24, comprenant, de plus, une couche tampon (154) formée entre l'électrode de grille (8, 25, 108, 155) et la couche isolante de grille (6, 27, 106, 153).

**26.** Dispositif optoélectronique incorporant un ou plusieurs composants selon l'une quelconque des revendications 14 à 25.

FIG. 1

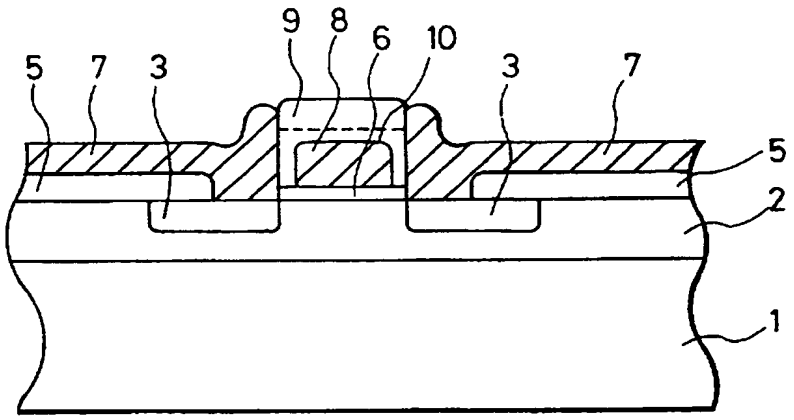

FIG. 2

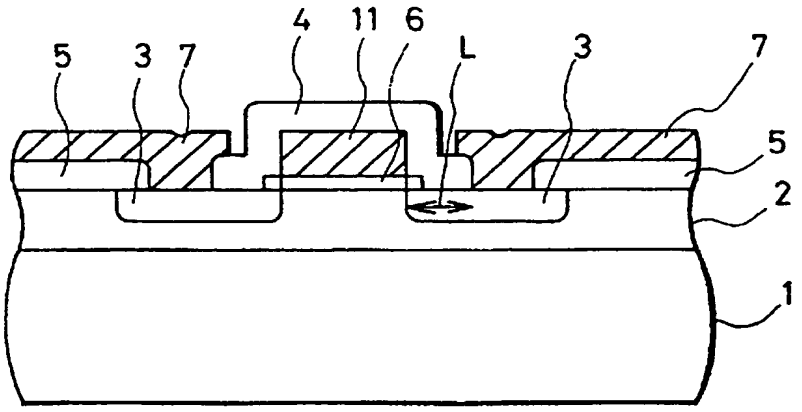

FIG. 3(A)

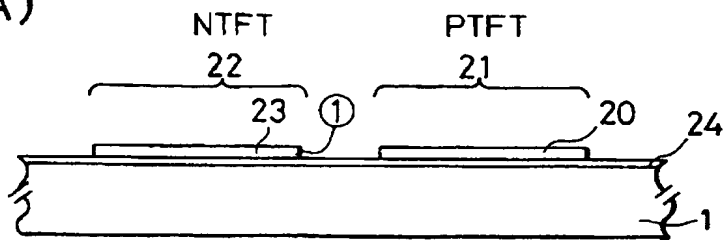


FIG. 3(B)

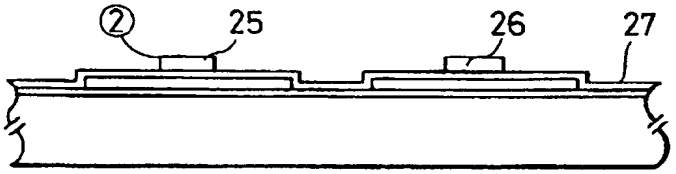


FIG. 3(C)

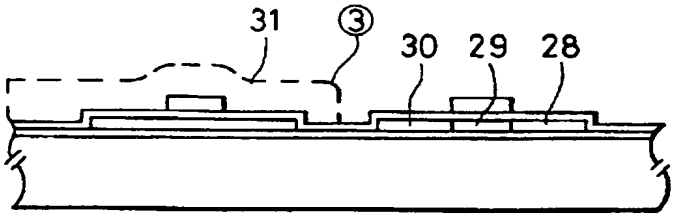


FIG. 3(D)

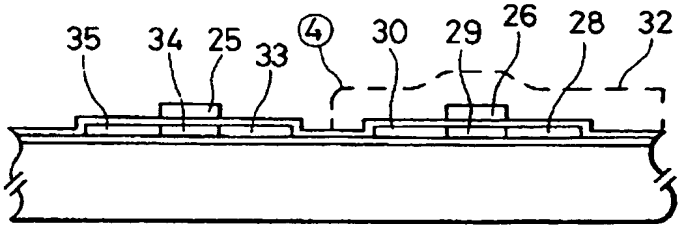

FIG. 3(E)

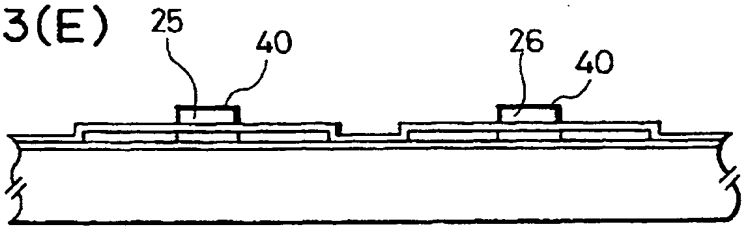


FIG. 3(F)

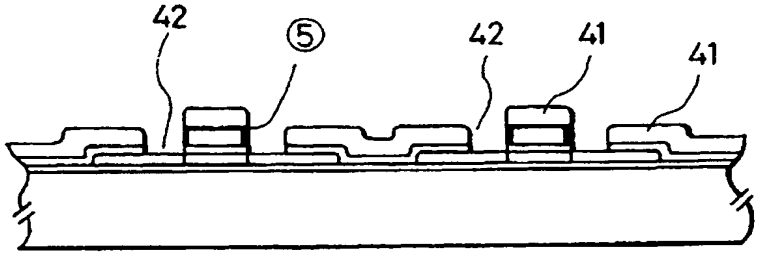


FIG. 3(G)

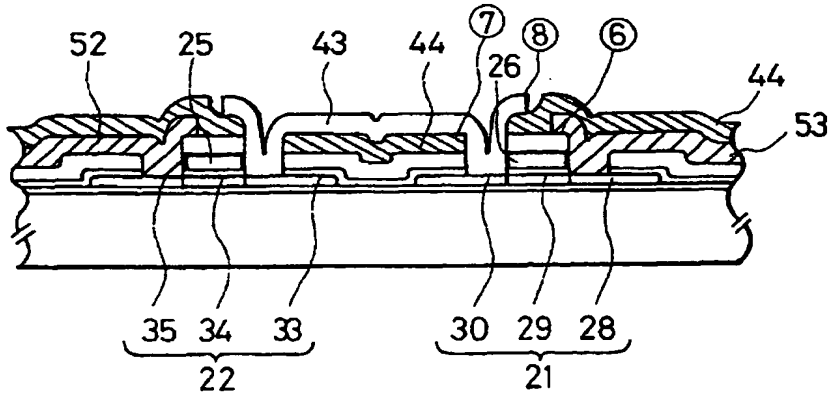

FIG. 4

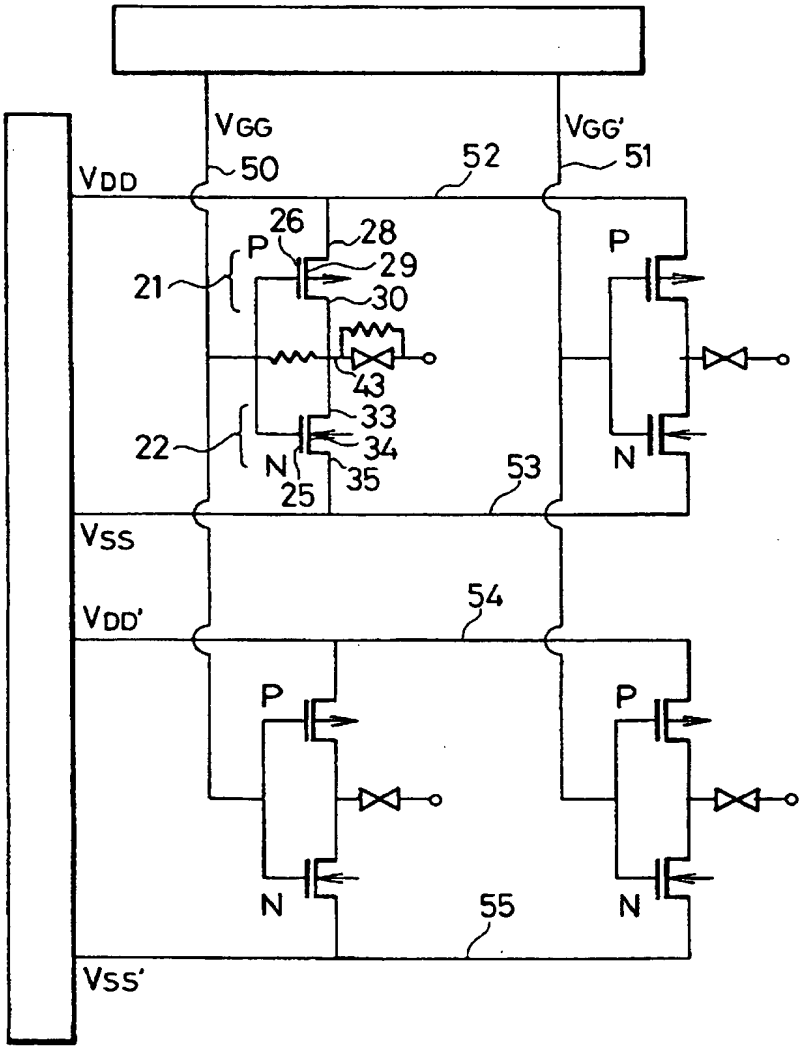
VGG
VGG'
50
52
51
VDD
26
28
P
29
21
30
43
33
22
34
N
25
35
53
VSS
VDD'
54
P
N
55
VSS'

FIG. 5

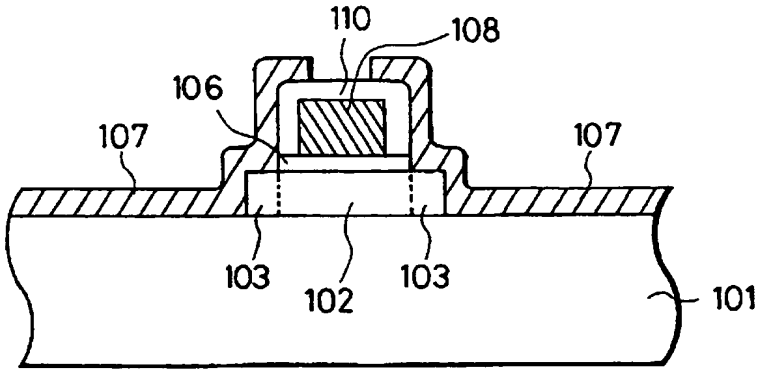

FIG. 6

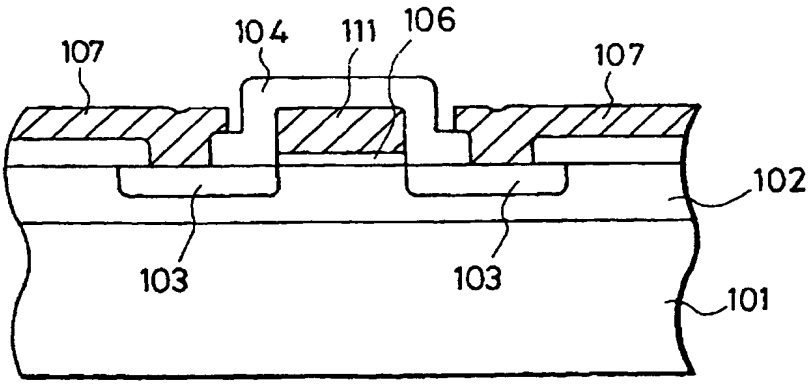

FIG. 7(A)

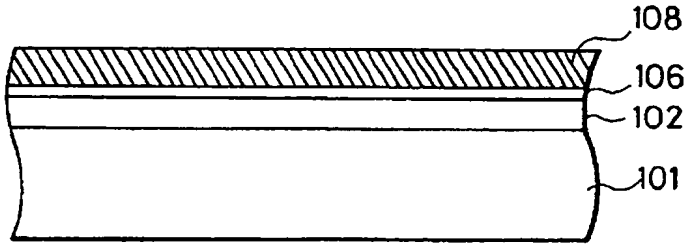


FIG. 7(B)

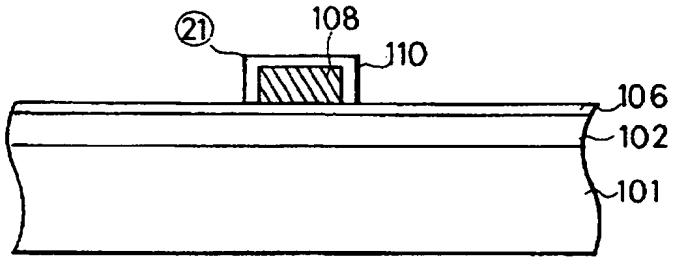


FIG. 7(C)

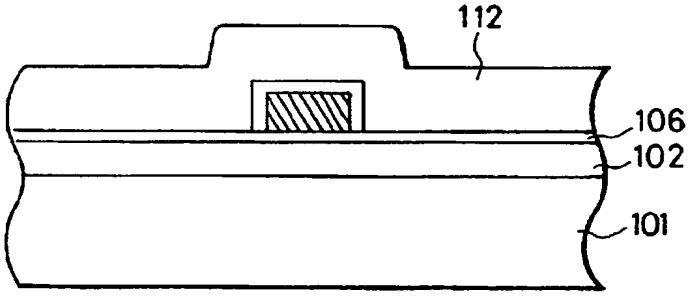


FIG. 7(D)

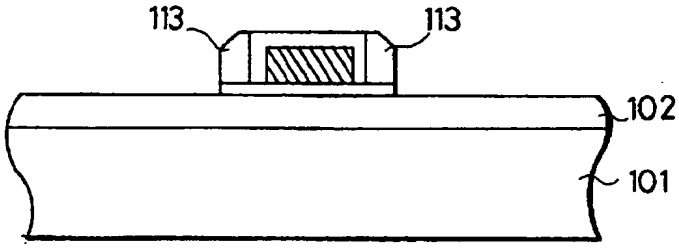

FIG. 7(E)

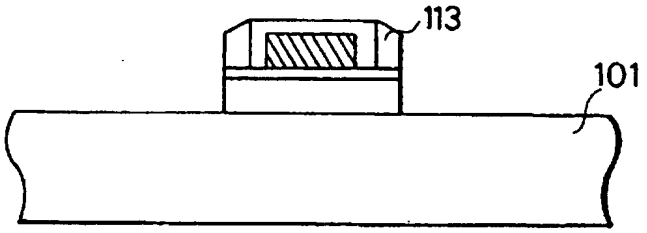


FIG. 7(F)

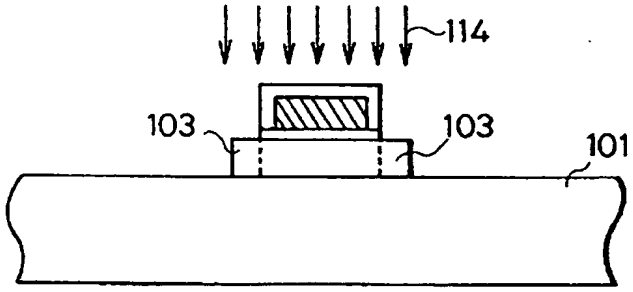


FIG. 7(G)

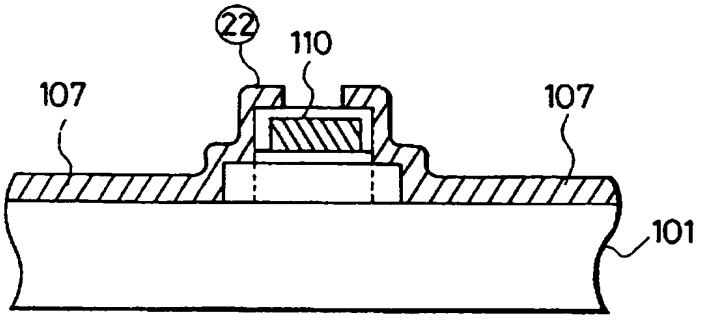

FIG. 8(A)

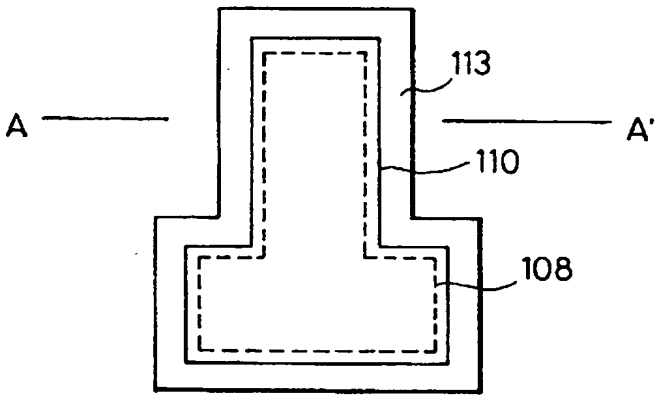


FIG. 8(B)

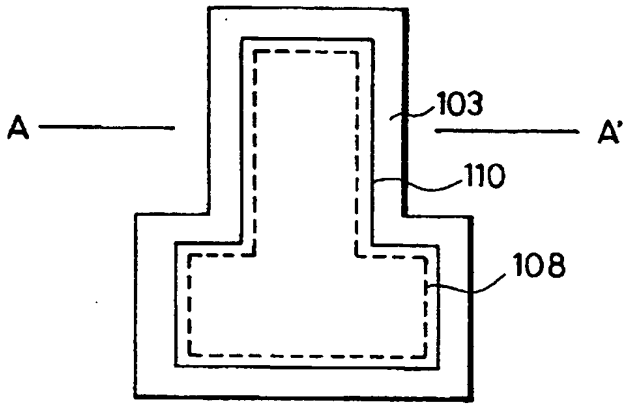

FIG. 8(C)

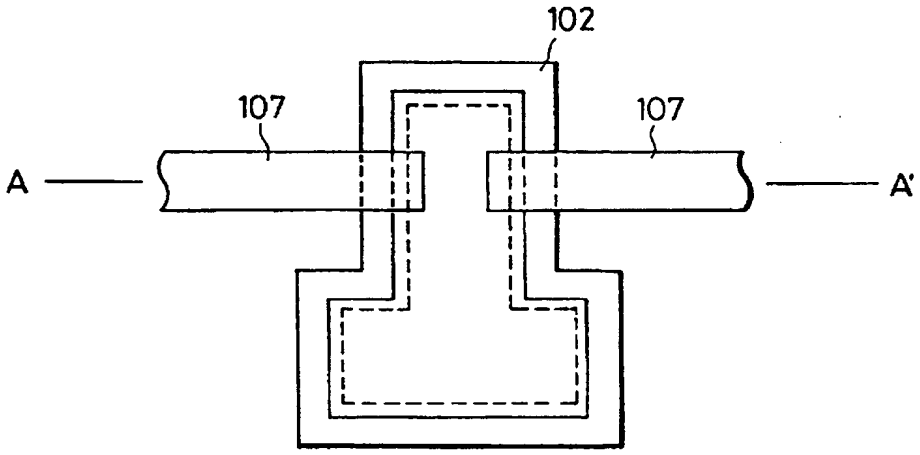


FIG. 8(D)

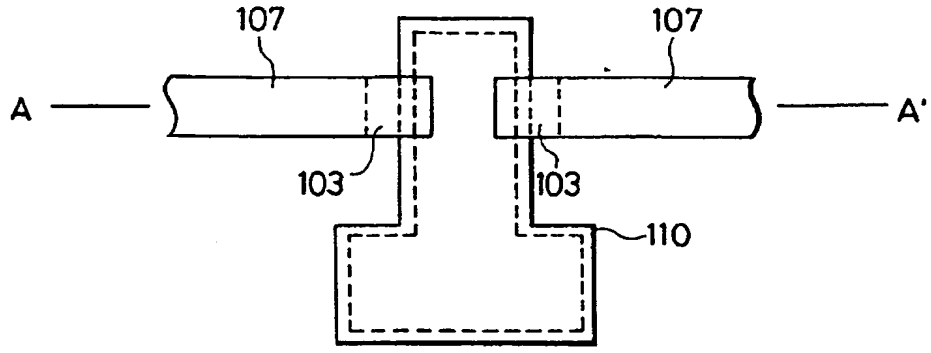

FIG. 9(A)

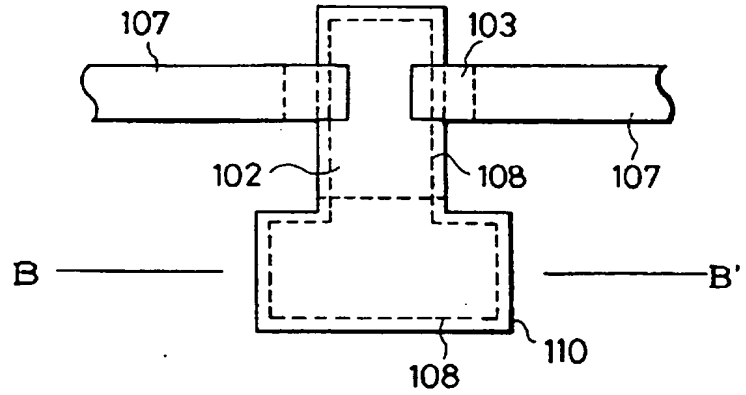


FIG. 9(B)

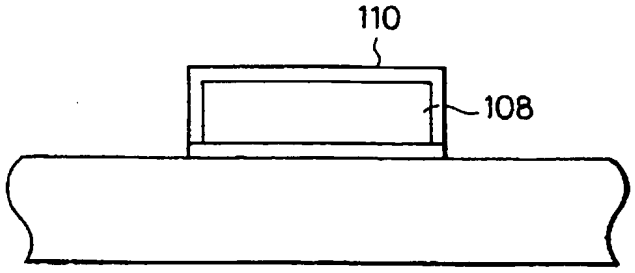

FIG. 10

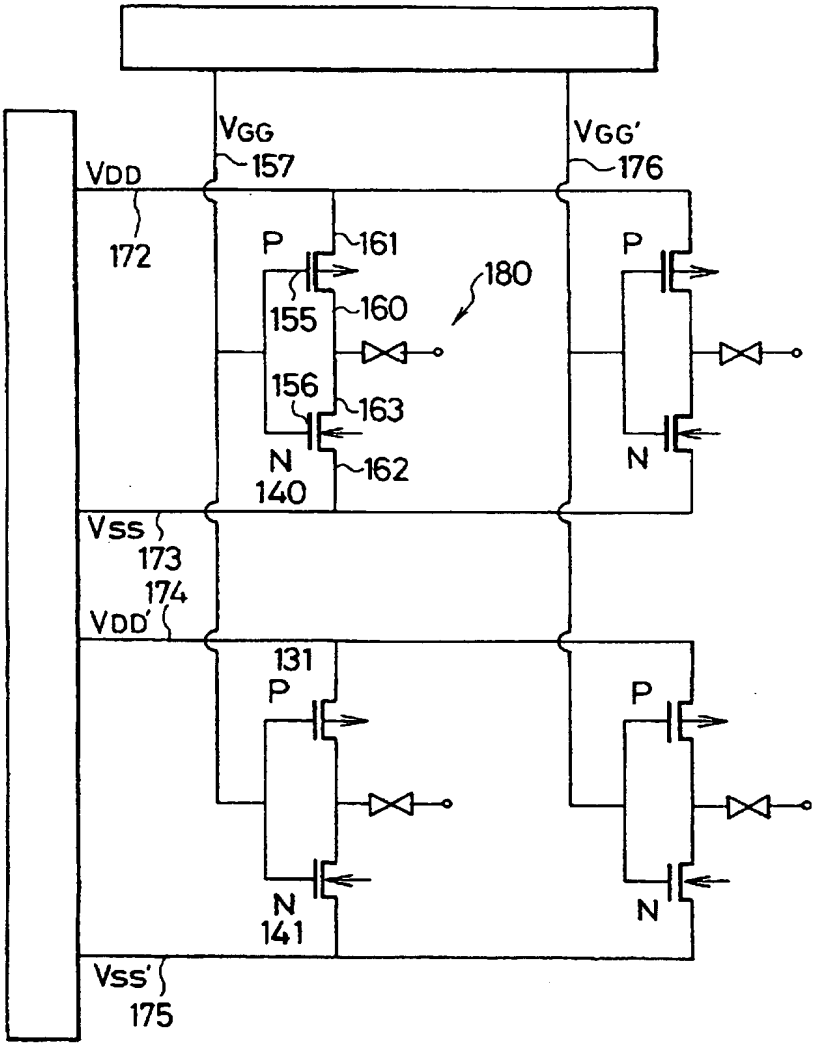
VGG
157
VGG'
176
VDD
172
P
161
180
155
160
156
163
N
162
140
P
N
Vss
173
174
VDD'
131
P
P
N
141
N
Vss'
175

FIG. 11(A)

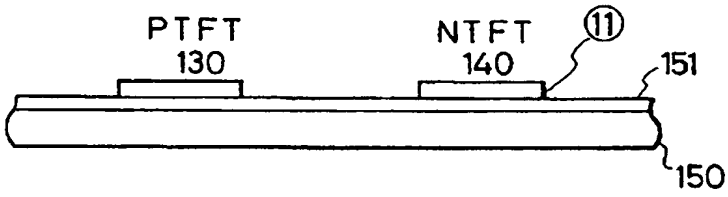


FIG. 11(B)

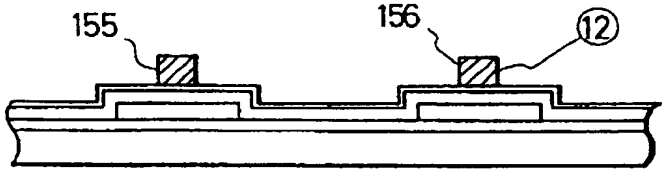


FIG. 11(C)

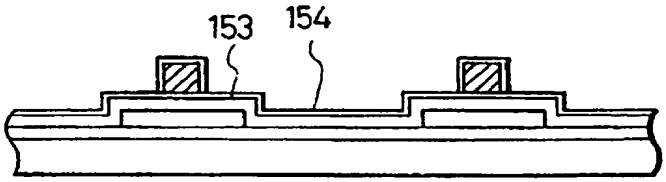


FIG. 11(D)

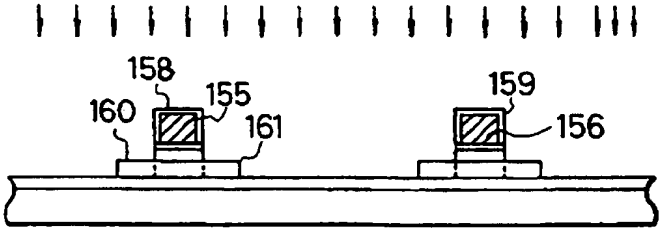


FIG. 11(E)

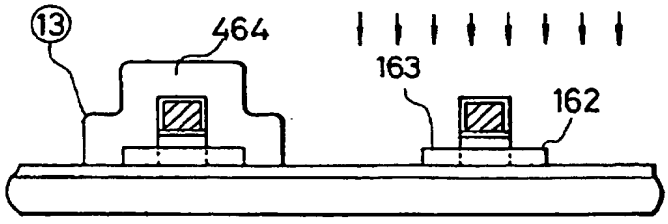

FIG. 11(F)

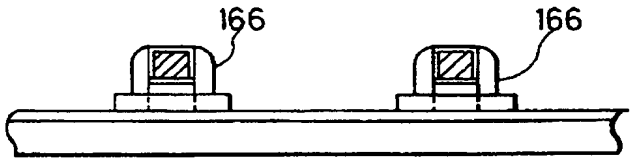


FIG. 11(G)

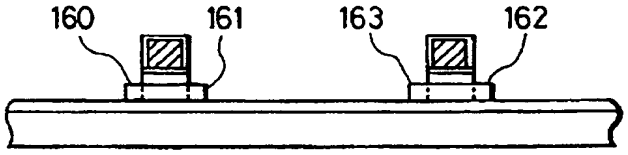


FIG. 11(H)

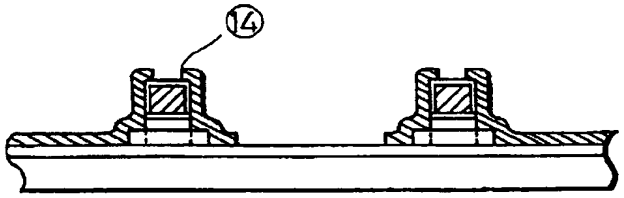


FIG. 11(I)

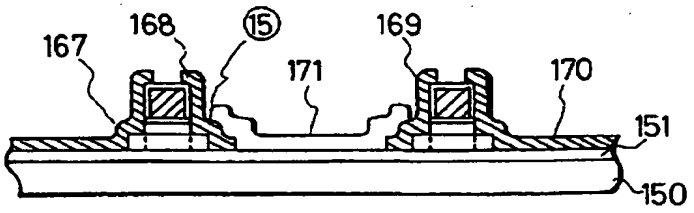

FIG. 12

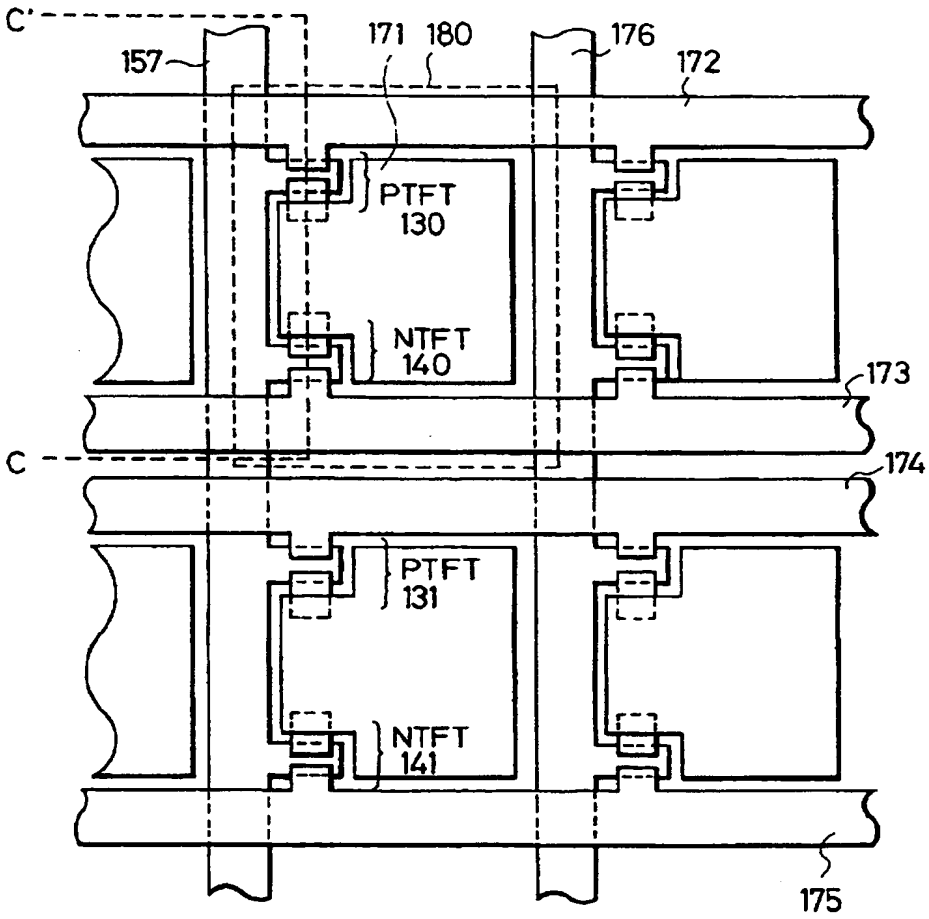
C'
157
171
180
176
172
PTFT
130
NTFT
140
173
C
174
PTFT
131
NTFT
141
175

FIG. 13

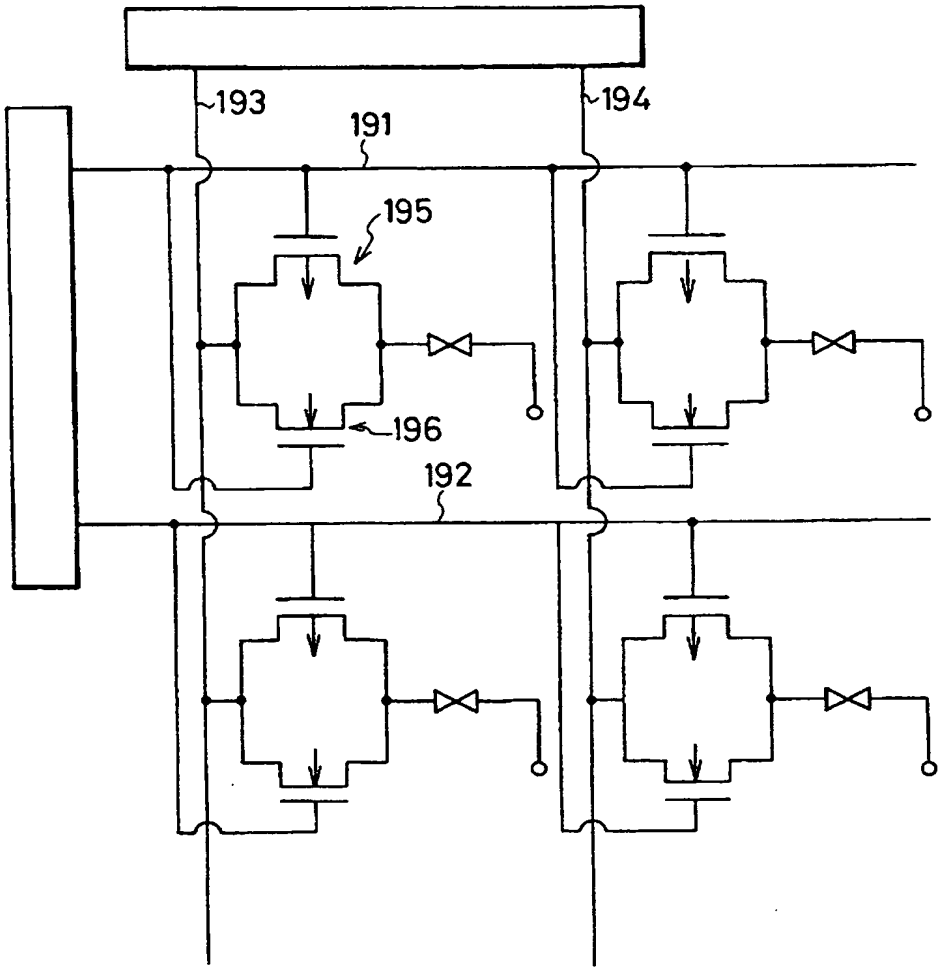

FIG. 14(A)

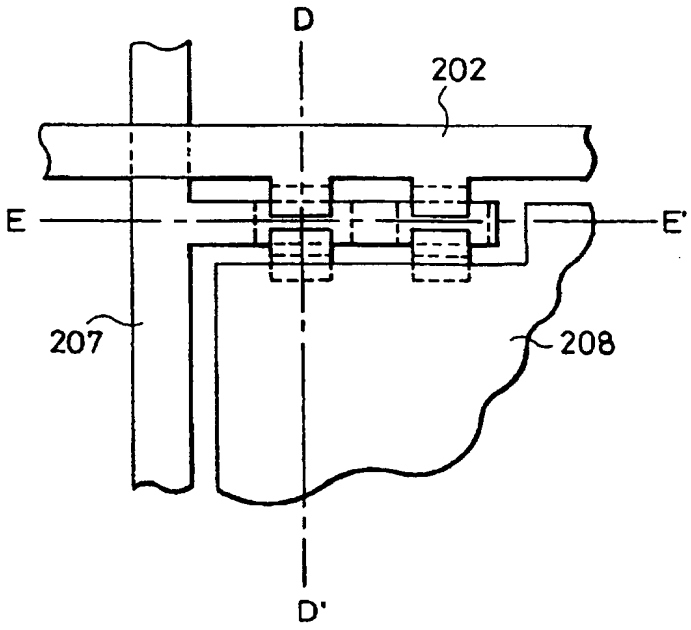


FIG. 14(B)

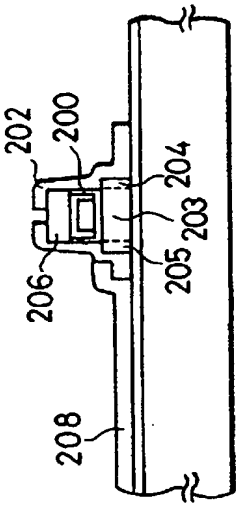


FIG. 14(C)